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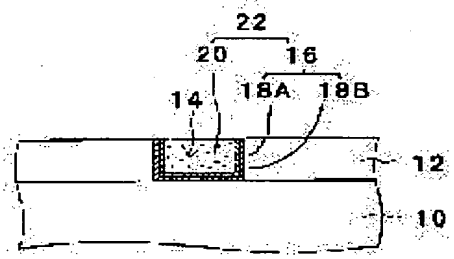
(54) WIRING STRUCTURE FOR SEMICONDUCTOR DEVICE, FORMATION OF WIRING AND THIN SILVER FILM, CVD SYSTEM AND CHEMICAL/ MECHANICAL POLISHING METHOD

(57)Abstract:
PURPOSE: To eliminate the patterning step for forming a wiring while solving the problems arising when an Al based alloy or Cu is employed as a wiring material.
CONSTITUTION: The wiring structure for a semiconductor device comprises (a). a trench 14 or an opening made in an insulation layer 12 formed on a substrate 10, and (b). a multilayer metal wiring layer 22 comprising a tight contact layer 16 and an Ag layer 20 formed in the trench 14 or the opening. The method for forming a wiring in a semiconductor device comprises a step for forming an insulation layer 12 on the substrate 10 and then making a trench 14 or an opening therein, a step for forming a multilayer metal wiring layer 22 comprising a tight contact layer 16 and an Ag layer 20 on the insulation film including the trench or the opening, and a step for removing the metal wiring layer 22 from above the insulation layer 12 while leaving the metal wiring layer 22 in the trench 14 or the opening.



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CLAIMS

[Claim(s)]
[Claim 1] (b) the multilayer metal wiring layer which consists of the adhesion layer from the bottom and Ag layer which were formed in the slot or opening formed in the insulating layer on a base, a (b) this slot, or opening circles -- since -- the wiring structure of the semiconductor device characterized by being constituted.
[Claim 2] Said adhesion layer is the two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or the wiring structure of the semiconductor device according to claim 1 characterized by consisting of the two-layer structure of Ag layer / Ti layer from the bottom.
[Claim 3] Wiring structure of the semiconductor device according to claim 1 or 2 characterized by forming the sidewall which changes from SiN to the side attachment wall of said slot or opening.
[Claim 4] (b) the process which forms a slot or opening in this insulating layer after forming an insulating layer on a base, and (**) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer and Ag layer on the insulating layer containing this slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leave a metal wiring layer to a slot or opening circles -- since -- the wiring formation approach of the semiconductor device characterized by to change.
[Claim 5] formation of said Ag layer -- Ag2 -- the wiring formation approach of the semiconductor device according to claim 4 characterized by being based on the chemistry gaseous-phase depositing method using CO3, AgNO2, AgBr, or AgI as a raw material.
[Claim 6] Removal of the metal wiring layer on the insulating layer in the process of the above (Ha) is the wiring formation approach of the semiconductor device according to claim 4 or 5 characterized by consisting of the chemical mechanical polish process of a metal wiring layer.
[Claim 7] The wiring formation approach of the semiconductor device according to claim 6 characterized by performing the chemical mechanical polish of Ag layer using the mixed water solution of I2 and KI.
[Claim 8] Removal of the metal wiring layer on the insulating layer in the process of the above (Ha) is the wiring formation approach of the semiconductor device according to claim 4 or 5 characterized by consisting of the etchback process of a metal wiring layer.
[Claim 9] Said adhesion layer is the wiring formation approach of a semiconductor device given in any 1 term of the two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer or claim 4 characterized by consisting of the two-layer structure of Ag layer / Ti layer from the bottom thru/or claim 8.
[Claim 10] The wiring formation approach of a semiconductor device given in any 1 term of claim 4 characterized by including further the process which forms the sidewall which changes from SiN to the side attachment wall of a slot or opening after the process of said (b) thru/or claim 9.

[Claim 11] (b) the multilayer metal wiring layer which consists of the adhesion layer from the bottom formed in the slot or opening formed in the insulating layer on a base, a (b) this slot, or opening circles, Cu layer, and Ag layer -- since -- the wiring structure of the semiconductor device characterized by being constituted.

[Claim 12] Said adhesion layer is the two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or the wiring structure of the semiconductor device according to claim 11 characterized by consisting of the two-layer structure of Ag layer / Ti layer from the bottom.

[Claim 13] Wiring structure of the semiconductor device according to claim 11 or 12 characterized by forming the sidewall which changes from SiN to the side attachment wall of said slot or opening.
[Claim 14] Wiring structure of the semiconductor device according to claim 11 or 12 characterized by forming the sidewall which changes from Ag to the side attachment wall of said slot or opening.
[Claim 15] (b) the process which forms a slot or opening in this insulating layer after forming an insulating layer on a base, and (**) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer, Cu layer, and Ag layer on the insulating layer containing this slot or opening circles, and the process which remove the metal wiring layer on an insulating layer (Ha), and leave a metal wiring layer to a slot or opening circles -- since -- the wiring formation approach of the semiconductor device characterized by to change.
[Claim 16] Removal of the metal wiring layer on the insulating layer in the process of the above (Ha) is the wiring formation approach of the semiconductor device according to claim 15 characterized by consisting of the chemical mechanical polish process of a metal wiring layer.
[Claim 17] The wiring formation approach of the semiconductor device according to claim 16 characterized by performing the chemical mechanical polish of Ag layer using the mixed water solution of I2 and KI.
[Claim 18] Removal of the metal wiring layer on the insulating layer in the process of the above (Ha) is the wiring formation approach of the semiconductor device according to claim 15 characterized by consisting of the etchback process of a metal wiring layer.
[Claim 19] (b) The process which forms a slot or opening in this insulating layer after forming an insulating layer on a base, The process which forms from the bottom the 1st multilayer metal wiring layer which consists of an adhesion layer and Cu layer on the insulating layer containing a (b) this slot or opening circles, The process which removes the 1st metal wiring layer on an insulating layer, and leaves the 1st metal wiring layer to a slot or opening circles, (Ha) the process which forms the 2nd metal wiring layer which consists of Ag layer on a (d) insulating layer and the 1st metal wiring layer, and the process which removes the 2nd metal wiring layer on a (e) insulating layer, and leaves the 2nd metal wiring layer to a slot or opening circles -- since -- the wiring formation approach of the semiconductor device characterized by changing.
[Claim 20] Removal of the 1st metal wiring layer on the insulating layer in the process of the above (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of said (e) is the wiring formation approach of the semiconductor device according to claim 19 characterized by consisting of a chemical mechanical polish process.
[Claim 21] The wiring formation approach of the semiconductor device according to claim 20 characterized by performing the chemical mechanical polish of Ag layer using the mixed water solution of I2 and KI.
[Claim 22] Removal of the 1st metal wiring layer on the insulating layer in the process of the above (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of said (e) is the wiring formation approach of the semiconductor device according to claim 19 characterized by consisting of an etchback process.
[Claim 23] Said adhesion layer is the wiring formation approach of a semiconductor device given in any 1 term of the two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer or claim 15 characterized by consisting of the two-layer structure of Ag layer / Ti layer from the bottom thru/or claim 22.
[Claim 24] The wiring formation approach of a semiconductor device given in any 1 term of claim 15 characterized by including further the process which forms the sidewall which changes from SiN to the side attachment wall of a slot or opening after the process of said (b) thru/or claim 23.
[Claim 25] The wiring formation approach of a semiconductor device given in any 1 term of claim

15 characterized by including further the process which forms the sidewall which changes from Ag to the side attachment wall of a slot or opening after the process of said (b) thru/or claim 23.

[Claim 26] The formation approach of the silver thin film by the chemistry gaseous-phase depositing method using Ag2CO3 as a raw material.
[Claim 27] The formation approach of the silver thin film by the chemistry gaseous-phase depositing method using AgNO2 as a raw material.
[Claim 28] The formation approach of the silver thin film by the chemistry gaseous-phase depositing method using AgBr as a raw material.
[Claim 29] The formation approach of the silver thin film by the chemistry gaseous-phase depositing method using AgI as a raw material.
[Claim 30] The CVD system which is a CVD system equipped with piping which connects the source of a raw material, a CVD chamber, and the source of a raw material and a CVD chamber, and is characterized by having the 1st heater which heats piping more than the boiling point of a raw material, and the 2nd heater which heats the CVD chamber induction for introducing a raw material into a CVD chamber more than the boiling point of a raw material.
[Claim 31] The 2nd heater is a CVD system according to claim 30 characterized by being lamp heating apparatus.
[Claim 32] The chemical mechanical polish method characterized by grinding a silver thin film chemically and mechanically using the mixed water solution of I2 and KI.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the CVD system suitable for formation of the wiring structure concerning the wiring structure of a semiconductor device where Ag (silver) was used as a wiring material and the wiring formation approach, the silver thin film formation approach, and a list, and the chemical mechanical polish method.
[0002]
[Description of the Prior Art] With high integration of a semiconductor device, the dimension Ruhr of the manufacture process of a semiconductor device makes it detailed, and is also making detailed wiring width of face in a semiconductor device in connection with this. Pure aluminium or an aluminium alloy (hereafter, these are named generically and it is also called aluminum system alloy) is mainly used as current and a wiring material. And after, forming the metal wiring layer which consists of aluminum system alloy by the so-called elevated-temperature aluminum spatter method for example, on the substrate which consists of an insulating layer, this metal wiring layer is made into a desired pattern configuration with a photolithography technique and an etching technique. Of this, wiring which consists of aluminum system alloy is formed. Then, an insulator layer is formed on wiring and flattening processing of this insulator layer is performed.
[0003] In order to form a resist pattern with a photolithography technique on a metal wiring layer, it is necessary to stop the scattered reflection of the light by the metal wiring layer at the time of exposure. When the scattered reflection of light is not stopped at the time of exposure, halation arises under the effect of the scattered reflection of light, and the defect of the stage piece of a resist etc. arises in the formed resist pattern. Therefore, regist patterning is performed after usually forming the antireflection film which consists of TiON on a metal wiring layer.
[0004] Hereafter, the example of a manufacture process of the conventional semiconductor device based on the elevated-temperature aluminum spatter method and the flattening approach by polish is explained with reference to drawing 20 , drawing 21 , and drawing 22 .
[0005] The component isolation region 102 and the gate field 104 are formed in the base 100 which consists of a [process -10] semi-conductor substrate. Then, a LDD ion implantation is performed, the gate sidewall 106 is formed, an ion implantation is performed and the source drain field 108 is formed (refer to (A) of drawing 20).
[0006] The layer insulation layer 112 is formed all over after that [[process -20]], and, subsequently to the layer insulation layer 112, opening 114 is formed (refer to (B) of drawing 20).
[0007] After forming the adhesion layer 116 which consists of Ti/TiN/Ti all over [a process -30], next the layer insulation layer 112 which contains opening 114 in a spatter, the metal wiring layer 118 which consists of aluminum system alloy (for example, aluminum-1wt%Si) by the elevated-temperature aluminum spatter method is made to deposit on the whole surface. Then, the antireflection film 120 which consists of TiON is formed in the whole surface. And wiring is formed by carrying out patterning of an antireflection film 120, the metal wiring layer 118, and the adhesion layer 116 with a photolithography technique and a dry etching technique (refer to

(C) of drawing 20).
[0008] [Process -40] Subsequently flattening processing by polish is performed. That is, the 1st insulator layer 122 which consists of SiO2 by the plasma-CVD method all over the layer insulation layer 112 including wiring is formed, the stopper layer 124 which consists of SiN by the plasma-CVD method on it is formed, and the 2nd insulator layer 126 which consists of thick SiO2 is further formed with a CVD method on it (refer to (A) of drawing 21).
[0009] The 2nd insulator layer 126 is ground from the upper part after that [[process -50]]. And it grinds until the stopper layer 124 appears as a polished surface (refer to (B) of drawing 21). In this way, the 1st insulator layer 122 by which flattening was carried out is formed after wiring.
[0010] Or the insulator layer by which flattening processing was carried out can also be formed at the following processes again instead of [the process -40] and [the process -50] using the stopper layer 124 which consists of SiN.
[0011] The insulator layer 130 which consists of SiO2 by the [process-40'] plasma-CVD method is formed.
[0012] After that [[process-50']], a resist 132 is formed on an insulator layer 130, and patterning of the resist 132 is carried out so that the heights of an insulator layer 130 may be exposed (refer to (A) of drawing 22).
[0013] A resist 132 is removed after etching [process-60'], next the heights of an insulator layer 130 (refer to (B) of drawing 22).
[0014] a part of insulator layer 130 which remained after that [[process-70']], without being etched -- 130A is ground and flattening of an insulator layer 130 is performed.
[0015]
[Problem(s) to be Solved by the Invention] If wiring makes it detailed, it will become difficult to form the wiring width of face made into the purpose with a sufficient controllability. In response to the effect of the irregularity of the layer insulation layer 112 which is a substrate, irregularity arises in the front face of the metal wiring layer 118. Moreover, it is easy to be ruined when the metal wiring layer 118 which consists of aluminum system alloy is formed by the elevated-temperature aluminum spatter method etc. (that is, irregularity is easy to be formed). It originates in these and the coverage of the antireflection film 120 in the crevice of the metal wiring layer 118 falls (for example, refer to (C) of drawing 20). In order for the reflection factor of the light in the part to fall, the scattered reflection of light arises, and it becomes impossible consequently, to form the target patterning configuration to the metal wiring layer 118 under the effect of halation etc. as a result.
[0016] Moreover, the wiring structure after regist patterning is the 120/metal wiring layer 118 of antireflection films which consists of a top to TiON. Dry etching performs patterning of the metal wiring layer 118 after regist patterning. In this case, BCl3 system gas is usually used as etching gas. However, etching by BCl3 system gas is only a chemical reaction, and it is impossible to etch the antireflection film 120 which consists of TiON by BCl3 system gas. So, it is necessary to etch the antireflection film 120 in a physical spatter operation.
[0017] Therefore, in case the metal wiring layer 118 which consists of aluminum system alloy is etched, it is necessary to change into chemical etching conditions from the etching conditions which have a spatter operation. However, when the thickness of the 120/metal wiring layer 118 of antireflection film is uneven, these etching serves as an ununiformity by modification of such etching conditions.
[0018] Furthermore, the approach explained at [the process -40] and [the process -50] using the stopper layer 124 which consists of SiN has the following troubles. That is, although the stopper layer 124 is used in case the 2nd insulator layer 126 which consists of SiO2 is ground, the selection ratio to polish of SiO2 and SiN is obtained three to about six. Therefore, it does not function as a stopper so that the stopper layer 124 which consists of SiN may perform the terminal point judging of polish, but the 1st insulator layer 122 may be ground too much. Namely, the 2nd insulator layer 126 cannot be ground with a sufficient controllability. Consequently, it has the problem that perfect flattening of the 1st insulator layer 122 cannot be attained.
[0019] And if spacing of wiring is thin in case between wiring is embedded by the 1st insulator

layer 122 which consists of SiO2 or SOG with a CVD method etc., the embedding of the 1st insulator layer 122 becomes inadequate, and it also has the problem that "** (void)" 122A occurs in the 1st insulator layer 122 during wiring (refer to drawing 23).
[0020] on the other hand -- SiN -- from -- changing -- a stopper -- a layer -- 124 -- not using -- [-- a process - 40 -- ' --] - [-- a process - 70 -- ' --] -- having explained -- an approach -- also setting -- an insulator layer -- 130 -- polish -- the time -- an insulator layer -- 130 -- polish -- a terminal point -- a judgment -- carrying out -- **** . For this reason, it has the problem of grinding an insulator layer 130 too much.
[0021] Thus, in manufacture of a detailed semiconductor device, after forming wiring, the conventional approach of forming a flat insulator layer on it has the above various troubles, and there is still no approach for solving these troubles effectively.
[0022] In the above-mentioned process, aluminum system alloy is used as a wiring material. In the metal wiring layer 118 which consists of aluminum system alloy, electromigration is a big problem. Moreover, at the time of the dry etching of the metal wiring layer 118, by the corrosion of a metal wiring layer, a void occurs in a metal wiring layer and the dependability fall of wiring is caused. As a result of the aluminum particle in the metal wiring layer 118 moving when a current is passed to wiring as detailed wiring-ization progresses especially, current concentration arises in the minute chip void generated in the metal wiring layer. Therefore, it was missing with electromigration and much more dependability fall of wiring is caused by compound operation of a void.
[0023] Using copper (Cu) as a wiring material as a way stage which solves this problem is proposed. However, there is no suitable etching approach of Cu and it has various problems -- that the workability of Cu is not good, and heat treatment in the furnace which contains oxygen several% that it is very easy to oxidize cannot be performed. The problem of workability forms a slot in an insulating layer, and after making Cu deposit on an insulating layer including this slot, it can avoid it by grinding Cu on an insulating layer chemically and mechanically by the chemical mechanical polish method. However, an effective means to prevent oxidation of the front face of Cu embedded in the slot is not known.
[0024] Therefore, the 1st purpose of this invention does not need to perform the patterning process of the metal wiring layer by the photolithography technique and dry etching technique for forming wiring. and the insulating layer which includes wiring, without grinding the insulator layer formed on wiring like before -- completeness -- it is in offering the wiring structure and the wiring formation approach of a new semiconductor device which make flattening possible and can solve the trouble at the time of using aluminum system alloy and Cu as a wiring material further.
[0025] The 2nd purpose of this invention is to offer the new silver thin film formation approach. Furthermore, the 3rd purpose of this invention is to provide the CVD system list suitable for application to this wiring structure and the wiring formation approach with the chemical mechanical polish method.
[0026]
[Means for Solving the Problem] the 1st voice of this invention for attaining the 1st above-mentioned purpose -- the multilayer metal wiring layer which consists of the adhesion layer from the bottom and Ag layer by which the wiring structure of the semiconductor device applied like was formed in the slot or opening formed in the insulating layer on a (b) base, a (b) slot, or opening circles -- since -- it is characterized by being constituted.
[0027] In the wiring structure of the semiconductor device concerning the 1st mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, in order to prevent oxidation of a metal wiring layer on the side attachment wall of a slot or opening, the sidewall which consists of SiN may be formed.
[0028] The wiring formation approach of the semiconductor device concerning the 1st mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, (**) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion

layer and Ag layer on the insulating layer containing a slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leaves a metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.
[0029] the 1st voice of this invention -- the wiring formation approach of the semiconductor device applied like -- setting -- formation of Ag layer -- Ag2 -- it can carry out by the chemistry gaseous-phase depositing method using CO3, AgNO2, AgBr, or AgI as a raw material. Removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of a chemical mechanical polish process of a metal wiring layer, or an etchback process of a metal wiring layer. the chemical mechanical polish method -- setting -- the mixed water solution of I2 and KI -- using -- the chemical mechanical polish of Ag layer -- it can carry out.
[0030] Moreover, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. The process which forms the sidewall which changes from SiN to the side attachment wall of a slot or opening after the process of (b) can be included further.
[0031] the 2nd voice of this invention for attaining the 1st above-mentioned purpose -- the multilayer metal wiring layer which consists of the adhesion layer from the bottom by which the wiring structure of the semiconductor device applied like was formed in the slot or opening formed in the insulating layer on a (b) base, a (b) slot, or opening circles, Cu layer, and Ag layer -- since -- it is characterized by being constituted.
[0032] In the wiring structure of the semiconductor device concerning the 2nd mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, SiN or the sidewall which consists of Ag again may be formed in the side attachment wall of a slot or opening.
[0033] The wiring formation approach of the semiconductor device concerning the 2nd mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, (**) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer, Cu layer, and Ag layer on the insulating layer containing a slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leaves a metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.
[0034] In the wiring formation approach of the semiconductor device concerning the 2nd mode of this invention, removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of chemical mechanical polish processes of a metal wiring layer. In this case, removal of Ag layer by the chemical mechanical polish is performed using the mixed water solution of I2 and KI. Or removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of etchback processes of a metal wiring layer again.
[0035] The wiring formation approach of the semiconductor device concerning the 3rd mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, The process which forms from the bottom the 1st multilayer metal wiring layer which consists of an adhesion layer and Cu layer on the insulating layer containing a (b) slot or opening circles, The process which removes the 1st metal wiring layer on an insulating layer, and leaves the 1st metal wiring layer to a slot or opening circles, (Ha) the process which forms the 2nd metal wiring layer which consists of Ag layer on a (d) insulating layer and the 1st metal wiring layer, and the process which removes the 2nd metal wiring layer on a (e) insulating layer, and leaves the 2nd metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.
[0036] the 3rd voice of this invention -- in the wiring formation approach of the semiconductor device applied like, removal of the 1st metal wiring layer on the insulating layer in the process of (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of (e) can consist of chemical mechanical polish processes. In this case, removal of Ag layer by the chemical mechanical polish is performed using the mixed water solution of I2 and KI. Or removal of the 1st metal wiring layer on the insulating layer in the process of (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of (e) can consist of etchback processes

again.
[0037] In the wiring formation approach of the semiconductor device concerning the 2nd or 3rd mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, the process which forms the sidewall which changes from SiN or Ag to the side attachment wall of a slot or opening after the process of (b) can be included further.
[0038] The formation approach of the silver thin film for attaining the 2nd above-mentioned purpose is characterized by depending Ag2CO3 on the chemistry gaseous-phase depositing method used as a raw material. Or it is characterized by being based on the chemistry gaseous-phase depositing method using AgNO2 as a raw material again. Furthermore, it is characterized by being based on the chemistry gaseous-phase depositing method using AgBr as a raw material. Furthermore, it is characterized by being based on the chemistry gaseous-phase depositing method using AgI as a raw material. These raw materials are gasified and it uses as CVD gas using carrier gas, such as inert gas.
[0039] The CVD system of this invention for attaining the 3rd above-mentioned purpose is equipped with piping which connects the source of a raw material, a CVD chamber, and the source of a raw material and a CVD chamber. And it is characterized by having the 1st heater which heats piping more than the boiling point of a raw material, and the 2nd heater which heats the CVD chamber induction for introducing a raw material into a CVD chamber more than the boiling point of a raw material. The 2nd heater can be used as lamp heating apparatus.
[0040] The chemical mechanical polish method for attaining the 3rd above-mentioned purpose is characterized by grinding a silver thin film chemically and mechanically using the mixed water solution of I2 and KI.
[0041]
[Function] The metal wiring layer is formed in a slot or opening circles in this invention. Such a metal wiring layer of a gestalt removes the metal wiring layer on an insulating layer, and since it is formed by leaving a metal wiring layer to a slot or opening circles, it does not need to perform patterning of the metal wiring layer formed on the insulating layer by the photolithography technique and the dry etching technique like the conventional technique. Moreover, since flattening processing by removal of the metal wiring layer on an insulating layer is performed, it is not necessary to perform flattening processing of the insulator layer formed on wiring like a Prior art.
[0042] Ag cannot oxidize easily due to elevated-temperature heat treatment. Although Ag also oxidizes, it decomposes into AgO->Ag+O at the temperature more than 100-degreeC. For this reason, AgO is not stable at the temperature of hundreds of degreeC, and the oxide of Ag is not maintained. Moreover, since a metal wiring layer is constituted from Ag, the problem of electromigration like aluminum system alloy is not generated. Therefore, stable wiring can be formed in the wiring structure or the wiring formation approach concerning the 1st mode of this invention.
[0043] In the wiring formation approach concerning the wiring structure or the 2nd or 3rd mode concerning the 2nd mode of this invention, since a metal wiring layer is constituted from an Ag layer and a Cu layer, the problem of electromigration like aluminum system alloy is not generated. And since the front face of Cu layer is covered with Ag layer, oxidation of Cu layer can be prevented.
[0044] Hereafter, with reference to a drawing, this invention is explained based on an example. In addition, in an example 1 - an example 6, the wiring formation approach concerning the wiring structure and the 1st mode of a semiconductor device concerning the 1st mode of this invention is explained. Moreover, in an example 7 - an example 12, the wiring formation approach concerning the wiring structure and the 2nd mode of a semiconductor device concerning the 2nd mode of this invention is explained. Furthermore, in an example 13 - an example 15, the wiring formation approach concerning the wiring structure and the 3rd mode of a semiconductor device concerning the 2nd mode of this invention is explained.
[0045] (Example 1) an example 1 - an example 6 -- the 1st voice of this invention -- the wiring structure of the semiconductor device applied like, and the 1st voice -- it is related with the

wiring formation approach which starts like. The wiring structure of an example 1 changes from the multilayer metal wiring layer 22 formed in the slot 14 where a semiconductor device is typical, and which was formed in the insulating layer 12 on a base 10, and the slot 14 to drawing 1 so that a sectional view may be shown in part. The metal wiring layer 22 consists of an adhesion layer 16 and an Ag layer 20 from the bottom. The adhesion layer 16 is the two-layer structure of Ti layer 18 A/TiN layer 18B from the bottom.
[0046] the wiring formation approach of an example 1 -- (**) -- the process which forms a slot 14 in an insulating layer 12 after forming an insulating layer 12 on a base 10, and (**) -- it consists of the process which forms from the bottom the multilayer metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20, and the process which remove the metal wiring layer 22 on an insulating layer (Ha) 12, and leave the metal wiring layer 22 in a slot 14 on an insulating layer 12 including the inside of a slot 14. Formation of the Ag layer 20 is based on the chemistry gaseous-phase depositing method for having used Ag2CO3 as a raw material. Moreover, removal of the metal wiring layer 22 on the insulating layer 12 in the process of (Ha) consists of the chemical mechanical polish process of the metal wiring layer 22 of having used the mixed water solution of I2 and KI. By operating as a stopper the insulating layer 12 which consists of SiO2, it becomes possible to set up the selection ratio of the metal wiring layer 22 and insulating layer 12 to a chemical mechanical polish to infinity.
[0047] Hereafter, with reference to typical drawing 2 which is sectional views a part, such as a semiconductor device, the wiring formation approach of an example 1 is explained concretely.
[0048] The insulating layer 12 which consists of SiO2 is formed on the base 10 which consists of [a process -100, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be carried out as follows.
Gas used : SiH4/O2/N2=250/250 / 100sccm substrate heating temperature: 420-degreeC pressure : 13.3Pa thickness : 0.8 micrometers [0049] A slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique after that [[process -110]] (refer to (A) of drawing 2). In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 2 . The conditions of dry etching can be carried out as follows.
Gas used : C4F8=50sccmRF power : 1200W pressure : 2Pa [0050] The adhesion layer 16 which consists of Ti layer 18 A/TiN layer 18B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -120] next (refer to (B) of drawing 2). The adhesion layer 16 can be formed on condition that the following.
Formation use gas 150 degreeC thickness of Ti layer 18A : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : : Formation use gas of 50nmTiN layer 18B : Ar/N2=40/70sccm power : 5kW pressure : 0.47Pa thickness : 70nm[0051] The silver (Ag) layer 20 is formed in the whole surface with a CVD method after that [[process -130]] (refer to (C) of drawing 2). Formation of the Ag layer 20 is based on the chemistry gaseous-phase depositing method for having used Ag2CO3 as a raw material. The conditions of CVD can be carried out as follows.
Raw material : Source temperature of Ag2CO3 raw material : 170-degreeC use gas : Ag2CO3/Ar/H2=10/25/1000sccm pressure : 2.6x103Pa substrate heating temperature: By this, the Ag layer 20 deposits on the 450-degreeC insulating layer 12 including the inside of a slot 14. The Ag layer 20 is formed of the following reaction.
Ag2CO3+H2->2Ag+CO2**+H2O** [0052] The CVD system of this invention shown in drawing 3 for formation of the Ag layer 20 was used. This CVD system is equipped with the piping 204 which connects the CVD chamber 200, the source 202 of a raw material, the source of a raw material, and a CVD chamber. And it has the 1st heater 206 which heats piping 204 more than the boiling point of a raw material, and the 2nd heater 210 which heats the CVD chamber induction 208 for introducing a raw material into a CVD chamber more than the boiling point of a raw material. The 2nd heater 210 is lamp heating apparatus, and the mirror 212 is formed. Moreover, the aperture 214 made from a quartz is formed in the part of the about 208 CVD chamber induction [which opposes the 2nd heater 210] piping 204. In addition, it is a heater for lamp heating apparatus for 216 to heat a base 10 and 218 to heat inert gas induction among drawing 3 , and for 220 heat the source 202 of a raw material. At the 1st and 2nd heaters

206,210, Ag2CO3 gas which flows the inside of piping 204 and the CVD chamber induction 208 is held more than 218-degreeC which is the boiling point.
[0053] By [a process -140], next the chemical mechanical polish method, the Ag layer 20 and the adhesion layer 16 on an insulating layer 12 are ground chemically and mechanically, and are removed, in a slot 14, it leaves the Ag layer 20 and the adhesion layer 16, and wiring which consists of the metal wiring layer 22 is formed (refer to drawing 1). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be carried out as follows.
Polish plate rotational frequency : 37rpm substrate maintenance base rotational frequency : 17rpm polishing pressure force : 5.5x108Pa pad temperature : A chemical mechanical polish is performed using the mixed water solution of 40 degreeCI2+KI.
[0054] since a slurry (abrasive material +KOH+ water of SiO2 system) is used when grinding SiO2 conventionally, but it is not distributed at homogeneity in the field which a slurry should grind in case SiO2 is ground by the slurry -- grinding -- passing -- etc. -- the problem that dispersion arises is in flattening of the polished surface in a substrate. When grinding the Ag layer 20 and the adhesion layer 16, a slurry is not needed, but by grinding with the mixed water solution of I2+KI, it is possible to remove only the Ag layer 20 and the adhesion layer 16, and it has the advantage that there is also little dispersion, in flattening of the polished surface in a substrate.
[0055] Wiring which consists of the metal wiring layer 22 embedded at the flat insulating layer 12 by this is formed. In an example 1, like the conventional wiring formation approach, regist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of regist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary.
[0056] (Example 2) In the example 1, the metal wiring layer 22 which consists of the Ag layer 20 and the adhesion layer 16 on an insulating layer 12 was removed by the chemical mechanical polish method. The metal wiring layer 22 is removed [in / instead / an example 2] by the etchback method by dry etching. In addition, other processes are the same as an example 1, and detailed explanation is omitted.
[0057] Etchback is carried out by the dry etching method of the following conditions, and it leaves the metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20 in a slot 14 for the Ag layer 20 and the adhesion layer 16 which were formed on the insulating layer 12 including the [etching process of metal wiring layer 22] slot 14.
Gas used : NO2/O2=20 / 20sccm microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : 100-degreeC [0058] (Example 3) In an example 3, the process which forms the sidewall 26 which changes from SiN to the side attachment wall of a slot 14 between the [process -110] of an example 1 and [a process -120] is included further. In addition, other processes are the same as an example 1, and detailed explanation is omitted.
Hereafter, the formation process of the sidewall 26 of an example 3 is explained with reference to drawing 5 . By forming a sidewall 26, oxidation of the adhesion layer 16 by the insulating layer 12 can be prevented.
[0059] SiN layer 26A is made to deposit by the plasma-CVD method the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall 26] slot 14 (refer to (A) of drawing 5). The formation conditions of SiN layer 26A are illustrated below.
Gas used: SiH4/NH3/N2=180/500/720sccm temperature : 200-degreeC pressure : 40Pa thickness : 100nm [0060] Then, whole surface etchback of the SiN layer 26A is carried out (refer to (B) of drawing 5). The conditions of etchback can be carried out as follows.
Gas used : CHF3=50sccmRF power : 300W pressure : 2Pa of sidewalls 26 is formed in the side attachment wall of a slot 14 of this. Henceforth, the wiring structure shown in (C) of drawing 5 can be formed through [process -120] - [a process -140]. [of an example 1]
[0061] (Example 4) The wiring structure of an example 4 typical to drawing 6 which shows a sectional view in part Opening 14A formed in 1st insulating-layer 12A on the base 10 which differ an example 1 and a little and consists of a semi-conductor substrate, It consists of metal

wiring layers 22 which consist of the adhesion layer 16 and the Ag layer 20 which were embedded at slot 14B formed in 2nd insulating-layer 12B formed on 1st insulating-layer 12A, and opening 14A and slot 14B. In this case, the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the flank of slot 14B may be formed. Moreover, a lower layer conductor layer (for example, source drain field 36) and the wiring 24 in slot 14B are electrically connected by embedding opening 14A by the metal wiring layer 22.
[0062] The wiring formation approaches of an example 4 differ an example 1 and a little, after they form slot 14B in 2nd insulating-layer 12B formed on 1st insulating-layer 12A in opening 14A again at 1st insulating-layer 12A on the base 10 which consists of a semi-conductor substrate beforehand, embed opening 14A and slot 14B by the metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20, and form wiring structure. The metal wiring layer 22 on 2nd insulating-layer 12B is removed by the chemical mechanical polish method. Hereafter, the wiring formation approach of an example 4 is explained with reference to typical drawing 7 and typical drawing 8 which are sectional views a part, such as a semiconductor device.
[0063] On the base 10 which consists of the semi-conductor substrate which consists of [Process] -400 Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, in order to form the gate sidewall 34 in the whole surface, SiO2 film is made to deposit, after performing a LDD ion implantation. The deposition conditions of SiO2 film can be carried out as follows.
Gas used : SiH4/O2-/N2=250/250 / 100sccm temperature : 420-degreeC pressure : 13.3Pa thickness : Further, whole surface etchback of SiO2 film is performed and 0.25 micrometers of gate sidewalls 34 are formed in the side attachment wall of the gate field 32. Whole surface etchback can be performed on condition that the following.
Gas used : C4F8=50sccmRF power: 1200W pressure : An impurity ion implantation is performed on condition that the following after that [2Pa] for formation of the source drain field 36. formation As of an N type channel Formation BF 2 of 20KeV and 5x1015-/cm2 P type channel 20KeV and 3x1015-/cm2 -- a part typical to (A) of drawing 7 in this way -- the structure shown with a sectional view can be acquired.
[0064] 1st insulating-layer 12A which consists of two-layer [of SiO2 and BPSG] is formed in the whole surface with the CVD method of the following conditions after that [[process -410]]. SiO two-layer formation use gas : TEOS 50sccm pressure : 40Pa temperature : 720-degreeC thickness : Formation use gas of 400nmBPSG layers : SiH4/PH3/B-2H6/O2/N2=80/7/7/1000/32000sccm temperature : 400-degreeC pressure : 1.0x105Pa thickness : 500nm 900 more degreeC and reflow processing for 20 minutes are performed, and flattening of 1st insulating-layer 12A is performed.
[0065] [A process -420], next 2nd insulating-layer 12B which consists of SiO2 are formed in the whole surface. 2nd insulating-layer 12B can be formed on condition that the following.
Gas used : SiH4/O2-/N2=250/250 / 100sccm temperature : 420-degreeC pressure : 13.3Pa thickness : 0.8 micrometers [0066] Slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -110] of an example 1 after that [[process -430]] (refer to (B) of drawing 7).
[0067] [Process -440] Subsequently opening 14A is formed in 1st insulating-layer 12A by performing dry etching after regist patterning (refer to (C) of drawing 7). Here, width of face of slot 14B is made larger than the path of opening 14A. The conditions of dry etching can be carried out as follows.
Gas used : C4F8 50sccmRF power: 1200W pressure : Further, 2Pa of 1100-degreeC and activation annealing for 10 seconds are performed, after forming a junction field by performing an ion implantation to opening circles. The following examples can be given as conditions for an ion implantation.
Formation As of an N type channel Formation BF 2 of 20KeV and 5x1015-/cm2 P type channel 20KeV, 3x1015-/cm2 [0068] It is desirable to form a SiN layer in the whole surface by the plasma-CVD method, to carry out whole surface etchback of the SiN layer subsequently like [the formation process of a sidewall 26] of an example 3, and to form the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the side attachment wall of

slot 14B after that [[process -450]], (refer to (A) of drawing 8).
[0069] The adhesion layer 16 which consists of Ti layer / TiN layer is formed in a spatter from under [a process -460] next on 2nd insulating-layer 12B containing opening 14A and slot 14B. This process can be made to be the same as that of the [process -120] of an example 1.
[0070] The Ag layer 20 is formed in the whole surface like the [process -130] of an example 1 after that [[process -470]] by the chemistry gaseous-phase depositing method using Ag2CO3 as a raw material (refer to (B) of drawing 8).
[0071] Like [a process -480], next the [process -140] of an example 1, by the chemical mechanical polish method, the Ag layer 20 and the adhesion layer 16 on 2nd insulating-layer 12B are ground chemically and mechanically, and are removed, in slot 14B and opening 14A, it leaves the Ag layer 20 and the adhesion layer 16, and the connection hole and wiring which consist of the metal wiring layer 22 are formed (refer to drawing 6). That is, the connection hole (for example, the so-called contact hole) with which the metal wiring layer 22 was embedded is formed in opening 14A. Moreover, the wiring 24 with which the metal wiring layer 22 was embedded at slot 14B is formed.
[0072] In addition, it is also removable by carrying out etchback by the dry etching method like an example 2 instead of removing the metal wiring layer 22 which consists of the Ag layer 20 and the adhesion layer 16 by the chemical mechanical polish method.
[0073] (Example 5) An example 5 is deformation of an example 4. Although the wiring structure of an example 5 is the same as an example 4, the wiring formation approach is different from an example 4. That is, opening 14A prepared in 1st insulating-layer 12A is embedded with the metal wiring material which consists of Ag, connection hole 24A is completed, subsequently to a it top, 2nd insulating-layer 12B is made to deposit, and the point which forms slot 14B in this 2nd insulating-layer 12B is different from an example 4. In an example 5, [the process -400], [a process -410], and [a process -440] of an example 4 are same process, and other processes differ. Hereafter, the approach of an example 5 is explained with reference to drawing 9 and drawing 10 .
[0074]
On the base 10 which consists of the semi-conductor substrate of [process -500] -[process -520] Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for formation of the source drain field 36. Then, 1st insulating-layer 12A which consists of two-layer [of SiO2 and BPSG] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed. Subsequently, activation annealing is performed after making a junction field form by forming opening 14A in 1st insulating-layer 12A in the dry etching after regist patterning, and performing an ion implantation to it at opening circles. These processes can be made to be the same as that of the [process -400] of an example 4, [a process -410], and [a process -440]. Subsequently, the sidewall (not shown) which consists of SiN may be formed in the side attachment wall of opening 14A.
[0075] [Process -530]
1st adhesion layer 16A which consists of Ti/TiN is formed in the whole surface from the bottom after [a process -520] by the same approach as the [process -120] of an example 1. Subsequently, by the same approach as the [process -130] of an example 1, 1st Ag layer 20A is formed on the whole surface with a CVD method, and the 1st metal wiring layer which consists of 1st adhesion layer 16A and 1st Ag layer 20A is formed (refer to (A) of drawing 9).
[0076] After that [[process -540]], the 1st metal wiring layer on 1st insulating-layer 12A is removed by the chemical mechanical polish method, and it leaves the 1st metal wiring layer 20A and 16A only in opening 14A (refer to (B) of drawing 9). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -140] of an example 1. Of this, the so-called contact hole 24A by which the 1st metal wiring layer was embedded at opening 14A is formed. Instead of the chemical mechanical polish method, it may leave the 1st metal wiring layer 20A and 16A only in opening 14A with the etchback by the dry etching method like an example 2.

[0077] [Process -550] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO2 is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -420] of an example 4. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -430] of an example 4 (refer to (A) of drawing 10). Then, if needed, a SiN layer may be formed in the whole surface by the plasma-CVD method, subsequently whole surface etchback of the SiN layer may be carried out like the [process -450] of an example 4, and the sidewall (not shown) which changes from SiN to the side attachment wall of slot 14B by this may be formed.
[0078] By the same approach as [a process -560], next the [process -120] of an example 1 After forming in a spatter 2nd adhesion layer 16B which consists of Ti with a thickness of 30nm on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -130] of an example 1 2nd Ag layer 20B is formed on the whole surface with a CVD method, and the 2nd metal wiring layer which consists of 2nd adhesion layer 16B and 2nd Ag layer 20B is formed.
[0079] [Process -570] Subsequently, by the chemical mechanical polish method, the 2nd metal wiring layer 20B and 16B on 2nd insulating-layer 12B is removed, in slot 14B, it leaves 2nd Ag layer 20B and 2nd adhesion layer 16B, and wiring 24 is formed (refer to (B) of drawing 10). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -140] of an example 1.
[0080] In addition, instead of removing the 2nd metal wiring layer 20B and 16B on 2nd insulating-layer 12B by the chemical mechanical polish method, like an example 2, etchback of the 2nd metal wiring layer 20B and 16B is carried out by the dry etching method, it can leave the 2nd metal wiring layer 20B and 16B only in slot 14B, and wiring 24 can also be formed in slot 14B by this.
[0081] (Example 6) An example 6 is deformation of an example 5. The point that an example 6 is different from an example 5 is in the point which forms a tungsten plug with a CVD method in opening 14A beforehand. Hereafter, the wiring formation approach of an example 6 is explained with reference to drawing 11 .
[0082]
[Process -600] - [a process -620] These processes can be made to be the same as that of [process -500] - [a process -520]. [of an example 5]
[0083] [Process -630]
The barrier layer 40 which consists of Ti/TiN is formed in the whole surface in a spatter after [a process -620], and the tungsten layer 42 is formed with a CVD method all over after that (refer to (A) of drawing 11). The membrane formation conditions of Ti and TiN can be made to be the same as that of the [process -120] of an example 1. Moreover, the membrane formation conditions of the tungsten by the CVD method are illustrated below.
Gas used : WF6/H2=95 / 550sccm membrane formation temperature : 450-degreeC pressure : 1.1x104Pa thickness : 0.4 micrometers [0084] After that [[process -640]], etchback is performed by the dry etching method, the tungsten layer 42 and the barrier layer 40 on 1st insulating-layer 12A are removed, and it leaves the metal plug and the barrier layer 40 which consist of the tungsten layer 42 only in opening 14A (refer to (B) of drawing 11). The conditions of dry etching can be carried out as follows.
Gas used : SF6=50sccm microwave power: 850WRF power : 150W pressure : Contact hole 24A which consists of the so-called tungsten plug by which the tungsten was embedded at opening 14A by this 1.33Pa is formed. In addition, it may leave the tungsten layer 42 and the barrier layer 40 only in opening 14A by the chemical mechanical polish method instead of the etchback by the dry etching method.
[0085] [Process -650] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO2 is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -550] of an example 5. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -550] of an example 5. In addition, width of face of slot 14B is made larger than the path of opening 14A.
[0086] After forming in a spatter the adhesion layer 16 which consists of Ti of 30nm thickness by the same approach as [a process -660], next the [process -560] of an example 5 on 2nd

insulating-layer 12B containing slot 14B, by the same approach as the [process -130] of an example 1, the Ag layer 20 is formed on the whole surface with a CVD method, and the metal wiring layer which consists of the adhesion layer 16 and the Ag layer 20 is formed.
[0087] The metal wiring layer on 2nd insulating-layer 12B is removed with the etchback by the chemical mechanical polish method or dry etching after that [[process -670]] by the same approach as the [process -140] of an example 1. By this, it leaves a metal wiring layer only in slot 14B, and the wiring 24 which consisted of metal wiring layers which consist of the adhesion layer 16 and the Ag layer 20 in slot 14B is formed (refer to (C) of drawing 11).
[0088] (Example 7) an example 7 - an example 12 -- the 2nd voice of this invention -- the wiring structure of the semiconductor device applied like, and the 2nd voice -- it is related with the wiring formation approach which starts like. The wiring structure of an example 7 changes from the multilayer metal wiring layer 50 formed in the slot 14 where a semiconductor device is typical, and which was formed in the insulating layer 12 on a base 10, and the slot 14 to drawing 12 so that a sectional view may be shown in part. The metal wiring layer 50 consists of an adhesion layer 52, a Cu layer 54, and an Ag layer 56 from the bottom. Moreover, the adhesion layer 52 is the two-layer structure of Ti layer 52 A/TiN layer 52B from the bottom.
[0089] the wiring formation approach of an example 7 -- (**) -- the process which forms a slot 14 in an insulating layer 12 after forming an insulating layer 12 on a base 10, and (**) -- it consists on an insulating layer 12 including a slot 14 of the process which forms from the bottom the multilayer metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56, and the process which removes the metal wiring layer 50 on an insulating layer (Ha) 12, and leaves a metal wiring layer in a slot 14.
[0090] Formation of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 is performed in a spatter. Moreover, removal of the metal wiring layer 50 on the insulating layer 12 in the process of (Ha) consists of the chemical mechanical polish process of the metal wiring layer 50. By operating as a stopper the insulating layer 12 which consists of SiO2, it becomes possible to set up the selection ratio of the metal wiring layer 50 and insulating layer 12 to a chemical mechanical polish to infinity.
[0091] Hereafter, with reference to typical drawing 13 which is sectional views a part, such as a semiconductor device, the wiring formation approach of an example 7 is explained concretely.
[0092] The insulating layer 12 which consists of SiO2 is formed on the base 10 which consists of [a process -700, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be made to be the same as that of the [process -100] of an example 1. Then, a slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique. In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 13 . The conditions of dry etching can be made to be the same as that of the [process -110] of an example 1.
[0093] The adhesion layer 52 which consists of Ti layer 52 A/TiN layer 52B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -710] next (refer to (A) of drawing 13). The adhesion layer 52 can be made to be the same as that of the [process -120] of an example 1.
[0094] The copper (Cu) layer 54 is formed in the whole surface in a spatter after that [[process -720]] (refer to (B) of drawing 13). The Cu layer 54 can be formed on the following spatter conditions.
Gas used : Ar=100sccm power : 10kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 500nm [0095] The silver (Ag) layer 56 is formed in the whole surface in a spatter after that [[process -730]] (refer to (C) of drawing 13). The Ag layer 56 can be formed in the spatter of the following conditions.
Gas used : Ar=100sccm power : 10kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 100nm of front faces of the Cu layer 54 is covered with the Ag layer 56 in this way.
[0096] By [a process -740], next the chemical mechanical polish method, the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on an insulating layer 12 are ground chemically and mechanically, and are removed, in a slot 14, it leaves the Ag layer 56, the Cu layer 54, and the

adhesion layer 52, and wiring which consists of the metal wiring layer 50 is formed (refer to drawing 12). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be carried out as follows.
Polish plate rotational frequency : 37rpm substrate maintenance base rotational frequency : 17rpm polishing pressure force : 5.5x108Pa pad temperature : The mixed water solution of I2+KI is used for removal by the chemical mechanical polish method of the 40-degreeCAg layer 56. Moreover, K4Fe(CN)6+H2O is used for removal by the chemical mechanical polish method of the Cu layer 54 and the adhesion layer 52.
[0097] since a slurry (abrasive material +KOH+ water of SiO2 system) is used when grinding SiO2 conventionally, but it is not distributed at homogeneity in the field which a slurry should grind in case SiO2 is ground by the slurry -- grinding -- passing -- etc. -- the problem that dispersion arises is in flattening of the polished surface in a substrate. When grinding the Ag layer 56, the Cu layer 54, and the adhesion layer 52, a slurry is not needed, but by grinding in the mixed water solution of I2+KI, and K4Fe(CN)6 water solution, it is possible to remove only the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and it has the advantage that there is also little dispersion, in flattening of the polished surface in a substrate.
[0098] Wiring which consists of the metal wiring layer 50 embedded at the flat insulating layer 12 by this is formed. In an example 7, like the conventional wiring formation approach, regist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of regist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary.
[0099] (Example 8) In the example 7, the metal wiring layer 50 which consists of the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on an insulating layer 12 was removed by the chemical mechanical polish method. The metal wiring layer 50 is removed [in / instead / an example 2] by the etchback method by dry etching. In addition, other processes are the same as an example 7, and detailed explanation is omitted.
[0100] Etchback is carried out by the dry etching method of the following conditions, and it leaves the metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 in a slot 14 for the Ag layer 56, the Cu layer 54, and the adhesion layer 52 which were formed on the insulating layer 12 including the [etching process of metal wiring layer 50] slot 14. The etching use gas of the Ag layer 56 : NO2/O2=20 / 20sccm microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : Etching use gas of the 100-degreeCCu layer 54 and the adhesion layer 52 : O2-/Cl2=10 / 70sccm microwave power: 1000WRF power : 300W pressure : 0.5Pa substrate heating temperature : 300-degreeC [0101] (Example 9) In an example 9, the process which forms the sidewall 26 which changes from SiN to the side attachment wall of a slot 14 between the [process -710] of an example 7 and [a process -720] is included further. In addition, other processes are the same as an example 7, and detailed explanation is omitted. Hereafter, the formation process of the sidewall 26 of an example 9 is explained with reference to drawing 14 . By forming a sidewall 26, oxidation of the adhesion layer 52 by the insulating layer 12 and the Cu layer 54 can be prevented.
[0102] SiN layer 26A is made to deposit by the plasma-CVD method the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall 26] slot 14 (refer to (A) of drawing 14). Next, whole surface etchback of the SiN layer 26A is carried out (refer to (B) of drawing 14). The formation conditions of SiN layer 26A and the conditions of etchback can be made to be the same as that of an example 3. A sidewall 26 is formed in the side attachment wall of a slot 14 of this. Henceforth, the wiring structure shown in (C) of drawing 14 can be formed through [process -720] - [a process -740]. [of an example 7]
[0103] (Example 10) The sidewall 26 which consists of SiN in an example 9 was formed in the side attachment wall of a slot 14. On the other hand, in an example 10, a sidewall is formed from Ag (silver). In addition, other processes are the same as an example 7, and detailed explanation is omitted. Hereafter, the formation process of the sidewall of an example 10 is explained. By forming the sidewall which consists of Ag, oxidation of the adhesion layer 52 by the insulating layer 12 and the Cu layer 54 can be prevented.

[0104] Ag layer is made to deposit in a spatter the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall which consists of Ag] slot 14. Next, whole surface etchback of the Ag layer is carried out. The formation conditions of Ag layer and the conditions of etchback are illustrated below.
Ag stratification condition use gas : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 100nmAg layer etchback condition use gas : NO2/O2=20 / 20sccm microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : 100degreeC -- the same sidewall can be formed in the side attachment wall of a slot 14 with having been shown in drawing 14 in this way. Henceforth, the same wiring structure can be formed with having been shown in (C) of drawing 14 through [process -720] - [a process -740]. [of an example 7]
[0105] (Example 11) The wiring structure of an example 11 typical to drawing 15 which shows a sectional view in part Opening 14A formed in 1st insulating-layer 12A on the base 10 which differ an example 7 and a little and consists of a semi-conductor substrate, It consists of metal wiring layers 50 which consist of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 which were embedded at slot 14B formed in 2nd insulating-layer 12B formed on 1st insulating-layer 12A, and opening 14A and slot 14B. In this case, the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the flank of slot 14B may be formed. Moreover, a lower layer conductor layer (for example, source drain field 36) and the wiring 58 in slot 14B are electrically connected by embedding opening 14A by the metal wiring layer 50.
[0106] The wiring formation approaches of an example 11 differ an example 7 and a little, after they form slot 14B in 2nd insulating-layer 12B formed on 1st insulating-layer 12A in opening 14A again at 1st insulating-layer 12A on the base 10 which consists of a semi-conductor substrate beforehand, embed opening 14A and slot 14B by the metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56, and form wiring structure. The metal wiring layer 50 on 2nd insulating-layer 12B is removed by the chemical mechanical polish method. Hereafter, the wiring formation approach of an example 11 is explained with reference to typical drawing 16 which is sectional views a part, such as a semiconductor device.
[0107] On the base 10 which consists of the semi-conductor substrate of [Process] -1100 Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for source drain field formation.
[0108] After that [[process -1110]], 1st insulating-layer 12A which consists of two-layer [of SiO2 and BPSG] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed.
[0109] [Process -1120] Subsequently to a 1st insulating-layer 12A top, 2nd insulating-layer 12B which consists of SiO2 is formed.
[0110] Slot 14B is formed in 2nd insulating-layer 12B after that [[process -1130]].
[0111] [Process -1140] Opening 14A is further formed in 1st insulating-layer 12A. Subsequently, activation annealing is performed after making a junction field form by performing an ion implantation to opening circles.
[0112] The above process can be made to be the same as that of [process -400] - [a process -440]. [of an example 4]
[0113] [Process -1150] Subsequently the sidewall 26 which consists of SiN may be formed in the side attachment wall of opening 14A and slot 14B like the [process -450] of an example 4. Of the above process, the structure shown in (A) of drawing 16 is formed.
[0114] The adhesion layer 52 which consists of Ti layer / TiN layer is formed in a spatter from under [a process -1160] next on 2nd insulating-layer 12B containing opening 14A and slot 14B. This process can be made to be the same as that of the [process -120] of an example 1.
[0115] The Cu layer 54 is formed in the whole surface in a spatter like the [process -720] of an example 7 after that [[process -1170]]. Subsequently, the Ag layer 56 is formed in the whole surface in a spatter like the [process -730] of an example 7 (refer to (B) of drawing 16).
[0116] After that [[process -1180]], like the [process -740] of an example 7, by the chemical mechanical polish method, the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on 2nd

insulating-layer 12B are ground chemically and mechanically, and are removed, in slot 14B and opening 14A, it leaves the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and the connection hole and wiring which consist of the metal wiring layer 50 are formed (refer to drawing 15). That is, connection hole 58A (for example, the so-called contact hole) where the metal wiring layer 50 was embedded is formed in opening 14A. Moreover, the wiring 58 with which the metal wiring layer 50 was embedded at slot 14B is formed.
[0117] In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the metal wiring layer 50 which consists of the Ag layer 56, the Cu layer 54, and the adhesion layer 52 by the chemical mechanical polish method.
[0118] (Example 12) An example 12 is deformation of an example 11. Although the wiring structure of an example 12 is the same as an example 11, the wiring formation approach is different from an example 11. That is, after embedding opening 14A prepared in 1st insulating-layer 12A with the metal wiring material which consists of Cu and completing connection hole 58A, 2nd insulating-layer 12B is made to deposit on it, and the point which forms slot 14B in this 2nd insulating-layer 12B is different from an example 11. In an example 12, [the process -1100], [a process -1110], and [a process -1140] of an example 11 are same process, and other processes differ. Hereafter, the approach of an example 12 is explained with reference to drawing 17 .
[0119]
On the base 10 which consists of the semi-conductor substrate of [process -1200] -[process -1220] Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for source drain field formation. Then, 1st insulating-layer 12A which consists of two-layer [of SiO2 and BPSG] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed. Subsequently, activation annealing is performed after making a junction field form by forming opening 14A in 1st insulating-layer 12A in the dry etching after regist patterning, and performing an ion implantation to it at opening circles. These processes can be made to be the same as that of the [process -1100] of an example 4, [a process -1110], and [a process -1140]. Subsequently, the sidewall (not shown) which consists of SiN may be formed in the side attachment wall of opening 14A.
[0120] [Process -1230]
1st adhesion layer 52A which consists of Ti/TiN is formed in the whole surface from the bottom after [a process -1220] by the same approach as the [process -710] of an example 7. Subsequently, by the same approach as the [process -720] of an example 7, 1st Cu layer 54A is formed on the whole surface in a spatter, and the 1st metal wiring layer which consists of 1st adhesion layer 52A and 1st Cu layer 54A is formed.
[0121] After that [[process -1240]], the 1st metal wiring layer on 1st insulating-layer 12A is removed by the chemical mechanical polish method, and it leaves the 1st metal wiring layer 54A and 52A only in opening 14A (refer to (A) of drawing 17). The conditions of a chemical mechanical polish can be made to be the same as that of the chemical mechanical polish of Cu layer of the [process -740] of an example 7. Of this, the so-called contact hole 58A by which the 1st metal wiring layer was embedded at opening 14A is formed. Instead of the chemical mechanical polish method, it may leave the 1st metal wiring layer 54A and 52A only in opening 14A with the etchback by the dry etching method like an example 8.
[0122] [Process -1250] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO2 is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -1120] of an example 11. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -1130] of an example 11. Then, subsequently it can form and be easy to form a SiN layer in the whole surface by the plasma-CVD method, to carry out whole surface etchback of the SiN layer, and to have the sidewall (not shown) which consists of SiN in the side attachment wall of slot 14B by this if needed, like the [process -1150] of an example 11.
[0123] By the same approach as [a process -1260], next the [process -710] of an example 7

After forming in a spatter 2nd adhesion layer 52B which consists of Ti with a thickness of 30nm on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -730] of an example 7 The 2nd metal wiring layer which consists of 2nd adhesion layer 52B, 2nd Cu layer 54B, and the Ag layer 56 is formed by forming 2nd Cu layer 54B on the whole surface in a spatter, and forming the Ag layer 56 in a spatter on it further.
[0124] [Process -1270] Subsequently, by the chemical mechanical polish method, the 2nd metal wiring layer 56, 54B, and 52B on 2nd insulating-layer 12B is removed, in slot 14B, it leaves the Ag layer 56, Cu layer of ** 2nd 54B, and 2nd adhesion layer 52B, and wiring 58 is formed (refer to (B) of drawing 18). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -740] of an example 7.
[0125] In addition, instead of removing the 2nd metal wiring layer 56, 54B, and 52B on 2nd insulating-layer 12B by the chemical mechanical polish method Like an example 8, etchback of the 2nd metal wiring layer 56, 54B, and 52B is carried out by the dry etching method, by this, it can leave the 2nd metal wiring layer 56, 54B, and 52B only in slot 14B, and wiring 58 can also be formed in slot 14B.
[0126] (Example 13) an example 7 - an example 12 -- setting -- the wiring structure of a semiconductor device -- the 2nd voice of this invention -- it formed by the wiring formation approach which starts like. On the other hand, the wiring structure of the semiconductor device in an example 13 - an example 15 is formed by the wiring formation approach concerning the 3rd mode of this invention.
[0127] The process which forms a slot 14 in an insulating layer 12 after the wiring formation approach of the semiconductor device of an example 13 forms an insulating layer 12 on the (b) base 10, The process which forms from the bottom 1st multilayer metal wiring layer 50A which consists of the adhesion layer 52 and the Cu layer 54 on the insulating layer 12 including the (b) slot 14, The process which removes 1st metal wiring layer 50A on an insulating layer 12, and leaves 1st metal wiring layer 50A in a slot 14, (Ha) It consists of the process which forms 2nd metal wiring layer 50B which consists of Ag layer on the (d) insulating layer 12 and 1st metal wiring layer 50A, and the process which removes 2nd metal wiring layer 50B on the (e) insulating layer 12, and leaves 2nd metal wiring layer 50B in a slot 14.
[0128] The adhesion layer 52, the Cu layer 54, and formation at metal wiring layer 50B to the 2nd are performed in a spatter. Moreover, removal of 2nd metal wiring layer 50B on the insulating layer 12 in the process of (e) changes from the chemical mechanical polish process of the metal wiring layer 50 to removal of 1st metal wiring layer 50A on the insulating layer 12 in the process of (Ha), and a list. By operating as a stopper the insulating layer 12 which consists of SiO2, it becomes possible to set up the selection ratio of the 1st [to a chemical mechanical polish], and 2nd metal wiring layers 50A and 50B, and an insulating layer 12 to infinity.
[0129] In the wiring formation approach concerning the 3rd mode of this invention, the Cu layer 54 can be covered with 2nd metal wiring layer 50B which consists of Ag layer much more more certainly than the wiring formation approach concerning the 2nd mode of this invention.
[0130] Hereafter, with reference to typical drawing 18 and typical drawing 19 which are sectional views a part, such as a semiconductor device, the wiring formation approach of an example 13 is explained concretely.
[0131] The insulating layer 12 which consists of SiO2 is formed on the base 10 which consists of [a process -1300, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be made to be the same as that of the [process -100] of an example 1. Then, a slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique. In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 18 . The conditions of dry etching can be made to be the same as that of the [process -110] of an example 1.
[0132] The adhesion layer 52 which consists of Ti layer 52 A/TiN layer 52B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -1310] next. The adhesion layer 52 can be made to be the same as that of the [process -120] of an example 1.
[0133] The copper (Cu) layer 54 is formed in the whole surface in a spatter after that [[process -1320]] (refer to (A) of drawing 18). Formation of the Cu layer 54 can be made to be the same

as that of the [process -720] of an example 7. In this way, 1st multilayer metal wiring layer 50A which consists of the adhesion layer 52 and the Cu layer 54 can be formed from the bottom on the insulating layer 12 including a slot 14.
[0134] By [a process -1330], next the chemical mechanical polish method, the Cu layer 54 and the adhesion layer 52 on an insulating layer 12 are ground chemically and mechanically, and are removed, and it leaves 1st metal wiring layer 50A which consists of the Cu layer 54 and the adhesion layer 52 in a slot 14 (refer to (B) of drawing 18). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be made to be the same as that of an example 13. K4Fe(CN)6+H2O is used for removal by the chemical mechanical polish method of the Cu layer 54 and the adhesion layer 52.
[0135] 2nd metal wiring layer 50B which consists of a silver (Ag) layer is formed in the whole surface in a spatter after that [[process -1340]] (refer to (A) of drawing 19). Formation of Ag layer can be made to be the same as that of the [process -730] of an example 13. In this way, the front face of 1st metal wiring layer 50A is covered with 2nd metal wiring layer 50B which consists of Ag layer.
[0136] By [a process -1350], next the chemical mechanical polish method, 2nd metal wiring layer 50B which consists of Ag layer on an insulating layer 12 is ground chemically and mechanically, and is removed, it leaves 2nd metal wiring layer 50B which consists of Ag layer in a slot 14, and wiring which consists of the 1st and 2nd metal wiring layers 50A and 50B is formed (refer to (B) of drawing 19). The conditions of a chemical mechanical polish can be made to be the same as that of an example 13. In addition, the mixed water solution of I2+KI is used for removal by the chemical mechanical polish method of Ag layer.
[0137] In an example 13, like the conventional wiring formation approach, regist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of regist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary. Moreover, since the front face of 1st metal wiring layer 50A is covered with 2nd metal wiring layer 50B much more certainly, oxidation of the Cu layer 54 which constitutes 1st metal wiring layer 50A can be prevented.
[0138] In an example 13, although 1st metal wiring layer 50A and 2nd metal wiring layer 50B were chiefly removed by the chemical mechanical polish method, it is also removable like an example 8 with the etchback by the dry etching method.
[0139] Moreover, formation of the sidewall explained in the wiring formation approach, and the example 9 or example 10 of the semiconductor device concerning the 3rd mode of this invention explained in the example 13 is also combinable. Furthermore, the wiring formation approach explained in the example 13 is also applicable instead of the Ag layer 56 in an example 11 or an example 12.
[0140] (Example 14) Only the flow of the process in the case of applying the wiring formation approach explained in the example 13 instead of the Ag layer 56 in an example 11 is explained below. In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the 1st and/or 2nd metal wiring layer by the chemical mechanical polish method.
[0141] Formation of the component isolation region to a [process -1400] base top, and a gate field. LDD ion implantation. Formation of a gate sidewall. The impurity ion implantation for source drain field formation.
[Process -1410] Formation and reflow processing of the 1st of an insulating layer which consist of two-layer [of SiO2 and BPSG].
[Process -1420] Formation of the 2nd insulating layer which consists of SiO2 to a 1st insulating-layer top.
Formation of the slot to the 2nd insulating layer of [a process -1430].
Formation of opening to the 1st insulating layer of [a process -1440].
Formation by the spatter to a 2nd insulating-layer top including opening and the slot of an adhesion layer which consist of a [process -1450] Ti layer / TiN layer.
Formation of Cu layer by the spatter to a [process -1460] adhesion layer top.

Removal of Cu layer on the 2nd insulating layer by the [process -1470] chemical mechanical polish.
Formation of the 2nd metal wiring layer which changes from Ag layer by the spatter to the whole [process -1470] surface.
Removal of the 2nd metal wiring layer on the 2nd insulating layer by the [process -1480] chemical mechanical polish method.
[0142] (Example 15) Only the flow of the process in the case of applying the wiring formation approach explained in the example 13 instead of the Ag layer 56 in an example 12 is explained below. In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the 1st and/or 2nd metal wiring layer by the chemical mechanical polish method.
[0143] Formation of the component isolation region to a [process -1500] base top, and a gate field. LDD ion implantation. Formation of a gate sidewall. The impurity ion implantation for source drain field formation.
[Process -1510] Formation and reflow processing of the 1st of an insulating layer which consist of two-layer [of SiO2 and BPSG].
Formation of opening to the 1st insulating layer of [a process -1520].
[Process -1530] Formation by the spatter of the 1st metal wiring layer which consists of the 1st adhesion layer to a 1st insulating-layer top, and 1st Cu layer.
Removal of the 1st metal wiring layer on the 1st insulating layer by the [process -1540] chemical mechanical polish method. By this, the so-called contact hole where the 1st metal wiring layer was embedded at opening is formed.
Formation of the 2nd insulating layer which consists of SiO2 all over [a process -1550].
Formation of the slot to the 2nd insulating layer.
[Process -1560] Formation by the spatter of the 2nd adhesion layer to a 2nd insulating-layer top, and Cu layer.
Removal of Cu layer on the 2nd insulating layer by the [process -1570] chemical mechanical polish, and the 2nd adhesion layer.
Formation of the 2nd metal wiring layer which changes from Ag layer by the spatter to the whole [process -1580] surface.
Removal of the 2nd metal wiring layer on the 2nd insulating layer by the [process -1590] chemical mechanical polish method.
[0144] As mentioned above, although this invention was explained based on the desirable example, this invention is not limited to these examples. The various ingredients and the conditions of having used in the example are instantiation, and can be changed suitably. Depending on the case, opening can be formed instead of Slots 14 and 14B.
[0145] Although the insulating layer was explained as what consists of the combination of SiO2 or SiO2, and BPSG chiefly, it can constitute from what carried out the laminating of well-known insulating materials, such as BPSG, PSG and BSG, AsSG, PbSG, SbSG, SOG, SiON, or SiN, or these insulating layers to instead of [these].
[0146] In an example 1 - an example 6, although formation of the Ag layer 20 was performed by the chemistry gaseous-phase depositing method for having used Ag2CO3 as a raw material instead, it can be performed by the chemistry gaseous-phase depositing method using AgNO2, AgBr, or AgI as a raw material. The CVD conditions in these cases and the heating conditions of the material gas which flows the inside of piping 204 and the CVD chamber induction 208 at the 1st and 2nd heaters 206,210 in the CVD system shown in drawing 3 are illustrated and combined with below, and a reaction formula is shown.
[0147] raw material: -- source temperature of AgNO2 raw material 450-degreeC gas heating condition: -- more than 140-degreeC -- reaction-formula : 2AgNO2+7H2->2Ag+2NH3**+4H2O** : 150-degreeC use gas : AgNO2/Ar/H2=10/25/1000sccm pressure : 2.6x103Pa substrate heating temperature : [0148] Raw material: Source temperature of an AgBr raw material : 450-degreeC use gas : AgBr/Ar/H2=10/75 / 1000sccm pressure : 2.6x103Pa substrate heating temperature: 500-degreeC gas heating conditions: It is power more than 434-degreeC. : 500W (plasma CVD).

Reaction formula : 2AgBr+H2->2Ag+2HBr** [0149] Raw material: Source temperature of an AgI raw material : 560-degreeC use gas : AgI/Ar/H2=10/100 / 1000sccm pressure : 2.6x103Pa substrate heating temperature: 600-degreeC gas heating conditions: It is power more than 552-degreeC. : 500W (plasma CVD)
Reaction formula : 2AgI+H2->2Ag+2HI** [0150] In an example 7 - an example 15, it can form with a CVD method instead of forming Cu layer and/or Ag layer in a spatter. The formation conditions of Cu layer by the CVD method are illustrated below.
Gas used : Cu (HFA)2/H2=10 / 1000sccm pressure : 2.6x103Pa substrate heating temperature: 350-degreeC power : It is the abbreviation for hexafluoro acetylacetonate in 500W, in addition HFA.
[0151] An adhesion layer can also consist of a Ti layer or a TiN layer instead of Ti layer / TiN layer. The formation conditions of the Ti layer or the TiN layer in this case can be made to be the same as that of the formation conditions of Ti layer 18A explained at the [process -120] of an example 1, and TiN layer 18B. Or an adhesion layer can also be made into the two-layer structure of Ag layer / Ti layer from the bottom again. In this case, Ag layer can be formed in the spatter of the following conditions. Moreover, the formation conditions of Ti layer can be made to be the same as that of the formation conditions of Ti layer 18A explained at the [process -120] of an example 1.
Spatter condition use gas of Ag layer : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 50nm [0152] TiON and TiW can also be used instead of TiN which constitutes an adhesion layer. Moreover, by the case, the sequence of formation of a slot, formation of a sidewall, and formation of an adhesion layer can be changed, and it can also consider as the order of formation of a slot, formation of an adhesion layer, and formation of a sidewall. Moreover, the metal layer or metallic-compounds layer which constitutes adhesion layers, such as Ti and TiN, can be formed by the forming-membranes methods, such as CVD.
[0153] The silicon layer formed on the various substrates for producing the various component sections, such as an insulating layer in which the MgO substrate, the GaAs substrate, superconducting transistor substrate, and lower layer wiring layer other than a silicon semi-conductor substrate or the semi-conductor substrate with which the source drain field was formed were formed as a base, and a gate electrode which needs to form a connection hole (a contact hole, a beer hall, through hole), and needs to form electrical installation, and a thin film transistor can be mentioned.
[0154] In an example 6, although the tungsten plug was formed in opening 14A using the so-called blanket tungsten CVD method, a tungsten plug may be instead formed in opening 14A with the so-called tungsten selection CVD method. The conditions in this case can be carried out as follows. Gas used : WF6/SiH4/H2/Ar=10/7/1000/10 sccm ** Whenever : 260-degreeC ** Force : 26Pa [0155] This invention is applicable to other semiconductor devices other than an MOS semiconductor device (for example, a bipolar transistor, CCD).
[0156] Various kinds of sputtering systems, such as a magnetron sputtering system, DC sputtering system, RF sputtering system, an ECR sputtering system, and a bias sputtering system that impresses substrate bias, can perform a spatter.
[0157] In the wiring structure concerning the 1st mode of this invention under Ag layer again the 2nd voice of this invention -- the wiring structure which starts like -- setting -- the bottom of Cu layer -- or -- again -- the wiring layer or connection hole under an adhesion layer -- refractory metals, such as Mo and Ti, -- Or a monolayer or various combination ******** can be formed for the silicide of TiW, ZrN, W, WC, TiC, other MoSi2 and WSi2, and TiSi2 grade etc.
[0158]
[Effect of the Invention] In this invention, the patterning process of the metal wiring layer by the photolithography technique and dry etching technique for forming wiring is unnecessary. Therefore, the scattered reflection of the light in the conventional photolithography technique, or the heterogeneity of etching and the problem of a corrosion in dry etching is avoidable.
[0159] Moreover, in production of a semiconductor device which has detailed wiring, flattening with a perfect insulating layer including wiring becomes possible, without performing formation of

the insulator layer formed on wiring like before, or polish of this insulator layer. since the conventional SiO2 system insulator layer was deficient in the selectivity in polish, the controllability of polish was scarce, but since the selectivity over an insulating layer is large, the controllability of polish is also boiled markedly and polish's of a metal wiring layer improves.
[0160] Furthermore, in order to leave a metal wiring layer only to a slot or opening circles, by adopting the etchback by the chemical mechanical polish method or the dry etching method, a Prior art can be used as it is fundamentally, and the manufacturing cost of a semiconductor device does not increase.
[0161] In addition, by forming a sidewall in a slot or opening circles, oxidation of a metal wiring layer can be prevented, moreover, by the metal wiring layer, it is stabilized and a slot or opening can be embedded.
[0162] In the wiring structure and the wiring formation approach concerning the 1st mode of this invention, since wiring structure is constituted from an Ag layer which has electromigration-proof nature from aluminum system alloy, the dependability of a semiconductor device improves conventionally. Furthermore, since resistance is lower than aluminum system alloy, Ag can expect the response speed of a semiconductor device.
[0163] In the wiring formation approach which starts the wiring structure concerning the 2nd mode of this invention, and a list at the 2nd and 3rd modes, since a metal wiring layer is constituted from a Cu layer which has electromigration-proof nature from aluminum system alloy, the dependability of a semiconductor device improves conventionally. Moreover, since the front face of Cu layer is covered with Ag layer, while preventing oxidation of Cu layer, wiring resistance can be kept low with the low resistance of Ag. Although Cu had the need for process limitation on problems, such as oxidation, conventionally, it becomes possible to use processes, such as heat treatment of an oxygen ambient atmosphere.
[0164] By the silver thin film formation approach of this invention, CVD of Ag becomes possible and the perfect embedding of Ag to a slot or opening becomes possible.
[0165] Furthermore, in the CVD system of this invention, since the source charging line to a CVD chamber and the connection of a CVD chamber can be held to high temperature, it is stabilized and material gas can be supplied.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application] This invention relates to the CVD system suitable for formation of the wiring structure concerning the wiring structure of a semiconductor device where Ag (silver) was used as a wiring material and the wiring formation approach, the silver thin film formation approach, and a list, and the chemical mechanical polish method.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] With high integration of a semiconductor device, the dimension Ruhr of the manufacture process of a semiconductor device makes it detailed, and is also making detailed wiring width of face in a semiconductor device in connection with this. Pure aluminium or an aluminium alloy (hereafter, these are named generically and it is also called aluminum system alloy) is mainly used as current and a wiring material. And after, forming the metal wiring layer which consists of aluminum system alloy by the so-called elevated-temperature aluminum spatter method for example, on the substrate which consists of an insulating layer, this metal wiring layer is made into a desired pattern configuration with a photolithography technique and an etching technique. Of this, wiring which consists of aluminum system alloy is formed. Then, an insulator layer is formed on wiring and flattening processing of this insulator layer is performed.
[0003] In order to form a resist pattern with a photolithography technique on a metal wiring layer, it is necessary to stop the scattered reflection of the light by the metal wiring layer at the time of exposure. When the scattered reflection of light is not stopped at the time of exposure, halation arises under the effect of the scattered reflection of light, and the defect of the stage piece of a resist etc. arises in the formed resist pattern. Therefore, regist patterning is performed after usually forming the antireflection film which consists of TiON on a metal wiring layer.
[0004] Hereafter, the example of a manufacture process of the conventional semiconductor device based on the elevated-temperature aluminum spatter method and the flattening approach by polish is explained with reference to drawing 20 , drawing 21 , and drawing 22 .
[0005] The component isolation region 102 and the gate field 104 are formed in the base 100 which consists of a [process -10] semi-conductor substrate. Then, a LDD ion implantation is performed, the gate sidewall 106 is formed, an ion implantation is performed and the source drain field 108 is formed (refer to (A) of drawing 20).
[0006] The layer insulation layer 112 is formed all over after that [[process -20]], and, subsequently to the layer insulation layer 112, opening 114 is formed (refer to (B) of drawing 20).
[0007] After forming the adhesion layer 116 which consists of Ti/TiN/Ti all over [a process -30], next the layer insulation layer 112 which contains opening 114 in a spatter, the metal wiring layer 118 which consists of aluminum system alloy (for example, aluminum-1wt%Si) by the elevated-temperature aluminum spatter method is made to deposit on the whole surface. Then, the antireflection film 120 which consists of TiON is formed in the whole surface. And wiring is formed by carrying out patterning of an antireflection film 120, the metal wiring layer 118, and the adhesion layer 116 with a photolithography technique and a dry etching technique (refer to (C) of drawing 20).
[0008] [Process -40] Subsequently flattening processing by polish is performed. That is, the 1st insulator layer 122 which consists of SiO2 by the plasma-CVD method all over the layer insulation layer 112 including wiring is formed, the stopper layer 124 which consists of SiN by the plasma-CVD method on it is formed, and the 2nd insulator layer 126 which consists of thick SiO2 is further formed with a CVD method on it (refer to (A) of drawing 21).
[0009] The 2nd insulator layer 126 is ground from the upper part after that [[process -50]].

And it grinds until the stopper layer 124 appears as a polished surface (refer to (B) of drawing 21). In this way, the 1st insulator layer 122 by which flattening was carried out is formed after wiring.

[0010] Or the insulator layer by which flattening processing was carried out can also be formed at the following processes again instead of [the process -40] and [the process -50] using the stopper layer 124 which consists of SiN.

[0011] The insulator layer 130 which consists of SiO2 by the [process-40'] plasma-CVD method is formed.

[0012] After that [[process-50']], a resist 132 is formed on an insulator layer 130, and patterning of the resist 132 is carried out so that the heights of an insulator layer 130 may be exposed (refer to (A) of drawing 22).

[0013] A resist 132 is removed after etching [process-60'], next the heights of an insulator layer 130 (refer to (B) of drawing 22).

[0014] a part of insulator layer 130 which remained after that [[process-70']], without being etched -- 130A is ground and flattening of an insulator layer 130 is performed.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] In this invention, the patterning process of the metal wiring layer by the photolithography technique and dry etching technique for forming wiring is unnecessary. Therefore, the scattered reflection of the light in the conventional photolithography technique, or the heterogeneity of etching and the problem of a corrosion in dry etching is avoidable.
[0159] Moreover, in production of a semiconductor device which has detailed wiring, flattening with a perfect insulating layer including wiring becomes possible, without performing formation of the insulator layer formed on wiring like before, or polish of this insulator layer. since the conventional SiO2 system insulator layer was deficient in the selectivity in polish, the controllability of polish was scarce, but since the selectivity over an insulating layer is large, the controllability of polish is also boiled markedly and polish's of a metal wiring layer improves.
[0160] Furthermore, in order to leave a metal wiring layer only to a slot or opening circles, by adopting the etchback by the chemical mechanical polish method or the dry etching method, a Prior art can be used as it is fundamentally, and the manufacturing cost of a semiconductor device does not increase.
[0161] In addition, by forming a sidewall in a slot or opening circles, oxidation of a metal wiring layer can be prevented, moreover, by the metal wiring layer, it is stabilized and a slot or opening can be embedded.
[0162] In the wiring structure and the wiring formation approach concerning the 1st mode of this invention, since wiring structure is constituted from an Ag layer which has electromigration-proof nature from aluminum system alloy, the dependability of a semiconductor device improves conventionally. Furthermore, since resistance is lower than aluminum system alloy, Ag can expect the response speed of a semiconductor device.
[0163] In the wiring formation approach which starts the wiring structure concerning the 2nd mode of this invention, and a list at the 2nd and 3rd modes, since a metal wiring layer is constituted from a Cu layer which has electromigration-proof nature from aluminum system alloy, the dependability of a semiconductor device improves conventionally. Moreover, since the front face of Cu layer is covered with Ag layer, while preventing oxidation of Cu layer, wiring resistance can be kept low with the low resistance of Ag. Although Cu had the need for process limitation on problems, such as oxidation, conventionally, it becomes possible to use processes, such as heat treatment of an oxygen ambient atmosphere.
[0164] By the silver thin film formation approach of this invention, CVD of Ag becomes possible and the perfect embedding of Ag to a slot or opening becomes possible.
[0165] Furthermore, in the CVD system of this invention, since the source charging line to a CVD chamber and the connection of a CVD chamber can be held to high temperature, it is stabilized and material gas can be supplied.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] If wiring makes it detailed, it will become difficult to form the wiring width of face made into the purpose with a sufficient controllability. In response to the effect of the irregularity of the layer insulation layer 112 which is a substrate, irregularity arises in the front face of the metal wiring layer 118. Moreover, it is easy to be ruined when the metal wiring layer 118 which consists of aluminum system alloy is formed by the elevated-temperature aluminum spatter method etc. (that is, irregularity is easy to be formed). It originates in these and the coverage of the antireflection film 120 in the crevice of the metal wiring layer 118 falls (for example, refer to (C) of drawing 20). In order for the reflection factor of the light in the part to fall, the scattered reflection of light arises, and it becomes impossible consequently, to form the target patterning configuration to the metal wiring layer 118 under the effect of halation etc. as a result.
[0016] Moreover, the wiring structure after regist patterning is the 120/metal wiring layer 118 of antireflection films which consists of a top to TiON. Dry etching performs patterning of the metal wiring layer 118 after regist patterning. In this case, BCl3 system gas is usually used as etching gas. However, etching by BCl3 system gas is only a chemical reaction, and it is impossible to etch the antireflection film 120 which consists of TiON by BCl3 system gas. So, it is necessary to etch the antireflection film 120 in a physical spatter operation.
[0017] Therefore, in case the metal wiring layer 118 which consists of aluminum system alloy is etched, it is necessary to change into chemical etching conditions from the etching conditions which have a spatter operation. However, when the thickness of the 120/metal wiring layer 118 of antireflection film is uneven, these etching serves as an ununiformity by modification of such etching conditions.
[0018] Furthermore, the approach explained at [the process -40] and [the process -50] using the stopper layer 124 which consists of SiN has the following troubles. That is, although the stopper layer 124 is used in case the 2nd insulator layer 126 which consists of SiO2 is ground, the selection ratio to polish of SiO2 and SiN is obtained three to about six. Therefore, it does not function as a stopper so that the stopper layer 124 which consists of SiN may perform the terminal point judging of polish, but the 1st insulator layer 122 may be ground too much. Namely, the 2nd insulator layer 126 cannot be ground with a sufficient controllability. Consequently, it has the problem that perfect flattening of the 1st insulator layer 122 cannot be attained.
[0019] And if spacing of wiring is thin in case between wiring is embedded by the 1st insulator layer 122 which consists of SiO2 or SOG with a CVD method etc., the embedding of the 1st insulator layer 122 becomes inadequate, and it also has the problem that "** (void)" 122A occurs in the 1st insulator layer 122 during wiring (refer to drawing 23).
[0020] on the other hand -- SiN -- from -- changing -- a stopper -- a layer -- 124 -- not using -- [-- a process - 40 -- ' --] - [-- a process - 70 -- ' --] -- having explained -- an approach -- also setting -- an insulator layer -- 130 -- polish -- the time -- an insulator layer -- 130 -- polish -- a terminal point -- a judgment -- carrying out -- **** . For this reason, it has the problem of grinding an insulator layer 130 too much.
[0021] Thus, in manufacture of a detailed semiconductor device, after forming wiring, the conventional approach of forming a flat insulator layer on it has the above various troubles, and

there is still no approach for solving these troubles effectively.
[0022] In the above-mentioned process, aluminum system alloy is used as a wiring material. In the metal wiring layer 118 which consists of aluminum system alloy, electromigration is a big problem. Moreover, at the time of the dry etching of the metal wiring layer 118, by the corrosion of a metal wiring layer, a void occurs in a metal wiring layer and the dependability fall of wiring is caused. As a result of the aluminum particle in the metal wiring layer 118 moving when a current is passed to wiring as detailed wiring-ization progresses especially, current concentration arises in the minute chip void generated in the metal wiring layer. Therefore, it was missing with electromigration and much more dependability fall of wiring is caused by compound operation of a void.
[0023] Using copper (Cu) as a wiring material as a way stage which solves this problem is proposed. However, there is no suitable etching approach of Cu and it has various problems -- that the workability of Cu is not good, and heat treatment in the furnace which contains oxygen several% that it is very easy to oxidize cannot be performed. The problem of workability forms a slot in an insulating layer, and after making Cu deposit on an insulating layer including this slot, it can avoid it by grinding Cu on an insulating layer chemically and mechanically by the chemical mechanical polish method. However, an effective means to prevent oxidation of the front face of Cu embedded in the slot is not known.
[0024] Therefore, the 1st purpose of this invention does not need to perform the patterning process of the metal wiring layer by the photolithography technique and dry etching technique for forming wiring. and the insulating layer which includes wiring, without grinding the insulator layer formed on wiring like before -- completeness -- it is in offering the wiring structure and the wiring formation approach of a new semiconductor device which make flattening possible and can solve the trouble at the time of using aluminum system alloy and Cu as a wiring material further.
[0025] The 2nd purpose of this invention is to offer the new silver thin film formation approach. Furthermore, the 3rd purpose of this invention is to provide the CVD system list suitable for application to this wiring structure and the wiring formation approach with the chemical mechanical polish method.

[Translation done.]

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MEANS

[Means for Solving the Problem] the 1st voice of this invention for attaining the 1st above-mentioned purpose -- the multilayer metal wiring layer which consists of the adhesion layer from the bottom and Ag layer by which the wiring structure of the semiconductor device applied like was formed in the slot or opening formed in the insulating layer on a (b) base, a (b) slot, or opening circles -- since -- it is characterized by being constituted.
[0027] In the wiring structure of the semiconductor device concerning the 1st mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, in order to prevent oxidation of a metal wiring layer on the side attachment wall of a slot or opening, the sidewall which consists of SiN may be formed.
[0028] The wiring formation approach of the semiconductor device concerning the 1st mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, (**) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer and Ag layer on the insulating layer containing a slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leaves a metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.
[0029] the 1st voice of this invention -- the wiring formation approach of the semiconductor device applied like -- setting -- formation of Ag layer -- Ag2 -- it can carry out by the chemistry gaseous-phase depositing method using CO3, AgNO2, AgBr, or AgI as a raw material. Removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of a chemical mechanical polish process of a metal wiring layer, or an etchback process of a metal wiring layer. the chemical mechanical polish method -- setting -- the mixed water solution of I2 and KI -- using -- the chemical mechanical polish of Ag layer -- it can carry out.
[0030] Moreover, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. The process which forms the sidewall which changes from SiN to the side attachment wall of a slot or opening after the process of (b) can be included further.
[0031] the 2nd voice of this invention for attaining the 1st above-mentioned purpose -- the multilayer metal wiring layer which consists of the adhesion layer from the bottom by which the wiring structure of the semiconductor device applied like was formed in the slot or opening formed in the insulating layer on a (b) base, a (b) slot, or opening circles, Cu layer, and Ag layer -- since -- it is characterized by being constituted.
[0032] In the wiring structure of the semiconductor device concerning the 2nd mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, SiN or the sidewall which consists of Ag again may be formed in the side attachment wall of a slot or opening.
[0033] The wiring formation approach of the semiconductor device concerning the 2nd mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, (**) -- the process

which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer, Cu layer, and Ag layer on the insulating layer containing a slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leaves a metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.
[0034] In the wiring formation approach of the semiconductor device concerning the 2nd mode of this invention, removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of chemical mechanical polish processes of a metal wiring layer. In this case, removal of Ag layer by the chemical mechanical polish is performed using the mixed water solution of I2 and KI. Or removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of etchback processes of a metal wiring layer again.
[0035] The wiring formation approach of the semiconductor device concerning the 3rd mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, The process which forms from the bottom the 1st multilayer metal wiring layer which consists of an adhesion layer and Cu layer on the insulating layer containing a (b) slot or opening circles, The process which removes the 1st metal wiring layer on an insulating layer, and leaves the 1st metal wiring layer to a slot or opening circles, (Ha) the process which forms the 2nd metal wiring layer which consists of Ag layer on a (d) insulating layer and the 1st metal wiring layer, and the process which removes the 2nd metal wiring layer on a (e) insulating layer, and leaves the 2nd metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.
[0036] the 3rd voice of this invention -- in the wiring formation approach of the semiconductor device applied like, removal of the 1st metal wiring layer on the insulating layer in the process of (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of (e) can consist of chemical mechanical polish processes. In this case, removal of Ag layer by the chemical mechanical polish is performed using the mixed water solution of I2 and KI. Or removal of the 1st metal wiring layer on the insulating layer in the process of (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of (e) can consist of etchback processes again.
[0037] In the wiring formation approach of the semiconductor device concerning the 2nd or 3rd mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, the process which forms the sidewall which changes from SiN or Ag to the side attachment wall of a slot or opening after the process of (b) can be included further.
[0038] The formation approach of the silver thin film for attaining the 2nd above-mentioned purpose is characterized by depending Ag2CO3 on the chemistry gaseous-phase depositing method used as a raw material. Or it is characterized by being based on the chemistry gaseous-phase depositing method using AgNO2 as a raw material again. Furthermore, it is characterized by being based on the chemistry gaseous-phase depositing method using AgBr as a raw material. Furthermore, it is characterized by being based on the chemistry gaseous-phase depositing method using AgI as a raw material. These raw materials are gasified and it uses as CVD gas using carrier gas, such as inert gas.
[0039] The CVD system of this invention for attaining the 3rd above-mentioned purpose is equipped with piping which connects the source of a raw material, a CVD chamber, and the source of a raw material and a CVD chamber. And it is characterized by having the 1st heater which heats piping more than the boiling point of a raw material, and the 2nd heater which heats the CVD chamber induction for introducing a raw material into a CVD chamber more than the boiling point of a raw material. The 2nd heater can be used as lamp heating apparatus.
[0040] The chemical mechanical polish method for attaining the 3rd above-mentioned purpose is characterized by grinding a silver thin film chemically and mechanically using the mixed water solution of I2 and KI.

[Translation done.]

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

OPERATION

[Function] The metal wiring layer is formed in a slot or opening circles in this invention. Such a metal wiring layer of a gestalt removes the metal wiring layer on an insulating layer, and since it is formed by leaving a metal wiring layer to a slot or opening circles, it does not need to perform patterning of the metal wiring layer formed on the insulating layer by the photolithography technique and the dry etching technique like the conventional technique. Moreover, since flattening processing by removal of the metal wiring layer on an insulating layer is performed, it is not necessary to perform flattening processing of the insulator layer formed on wiring like a Prior art.
[0042] Ag cannot oxidize easily due to elevated-temperature heat treatment. Although Ag also oxidizes, it decomposes into AgO->Ag+O at the temperature more than 100-degreeC. For this reason, AgO is not stable at the temperature of hundreds of degreeC, and the oxide of Ag is not maintained. Moreover, since a metal wiring layer is constituted from Ag, the problem of electromigration like aluminum system alloy is not generated. Therefore, stable wiring can be formed in the wiring structure or the wiring formation approach concerning the 1st mode of this invention.
[0043] In the wiring formation approach concerning the wiring structure or the 2nd or 3rd mode concerning the 2nd mode of this invention, since a metal wiring layer is constituted from an Ag layer and a Cu layer, the problem of electromigration like aluminum system alloy is not generated. And since the front face of Cu layer is covered with Ag layer, oxidation of Cu layer can be prevented.
[0044] Hereafter, with reference to a drawing, this invention is explained based on an example. In addition, in an example 1 - an example 6, the wiring formation approach concerning the wiring structure and the 1st mode of a semiconductor device concerning the 1st mode of this invention is explained. Moreover, in an example 7 - an example 12, the wiring formation approach concerning the wiring structure and the 2nd mode of a semiconductor device concerning the 2nd mode of this invention is explained. Furthermore, in an example 13 - an example 15, the wiring formation approach concerning the wiring structure and the 3rd mode of a semiconductor device concerning the 2nd mode of this invention is explained.
[0045] (Example 1) an example 1 - an example 6 -- the 1st voice of this invention -- the wiring structure of the semiconductor device applied like, and the 1st voice -- it is related with the wiring formation approach which starts like. The wiring structure of an example 1 changes from the multilayer metal wiring layer 22 formed in the slot 14 where a semiconductor device is typical, and which was formed in the insulating layer 12 on a base 10, and the slot 14 to drawing 1 so that a sectional view may be shown in part. The metal wiring layer 22 consists of an adhesion layer 16 and an Ag layer 20 from the bottom. The adhesion layer 16 is the two-layer structure of Ti layer 18 A/TiN layer 18B from the bottom.
[0046] the wiring formation approach of an example 1 -- (**) -- the process which forms a slot 14 in an insulating layer 12 after forming an insulating layer 12 on a base 10, and (**) -- it consists of the process which forms from the bottom the multilayer metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20, and the process which remove the metal wiring layer 22 on an insulating layer (Ha) 12, and leave the metal wiring layer 22 in a slot 14 on

an insulating layer 12 including the inside of a slot 14. Formation of the Ag layer 20 is based on the chemistry gaseous-phase depositing method for having used Ag2CO3 as a raw material. Moreover, removal of the metal wiring layer 22 on the insulating layer 12 in the process of (Ha) consists of the chemical mechanical polish process of the metal wiring layer 22 of having used the mixed water solution of I2 and KI. By operating as a stopper the insulating layer 12 which consists of SiO2, it becomes possible to set up the selection ratio of the metal wiring layer 22 and insulating layer 12 to a chemical mechanical polish to infinity.

[0047] Hereafter, with reference to typical drawing 2 which is sectional views a part, such as a semiconductor device, the wiring formation approach of an example 1 is explained concretely.

[0048] The insulating layer 12 which consists of SiO2 is formed on the base 10 which consists of [a process -100, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be carried out as follows.

Gas used : SiH4/O2/N2=250/250 / 100sccm substrate heating temperature: 420-degreeC pressure : 13.3Pa thickness : 0.8 micrometers [0049] A slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique after that [[process -110]] (refer to (A) of drawing 2). In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 2 . The conditions of dry etching can be carried out as follows.

Gas used : C4F8=50sccmRF power : 1200W pressure : 2Pa [0050] The adhesion layer 16 which consists of Ti layer 18 A/TiN layer 18B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -120] next (refer to (B) of drawing 2). The adhesion layer 16 can be formed on condition that the following.

Formation use gas 150 degreeC thickness of Ti layer 18A : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : : Formation use gas of 50nmTiN layer 18B : Ar/N2=40/70sccm power : 5kW pressure : 0.47Pa thickness : 70nm[0051] The silver (Ag) layer 20 is formed in the whole surface with a CVD method after that [[process -130]] (refer to (C) of drawing 2). Formation of the Ag layer 20 is based on the chemistry gaseous-phase depositing method for having used Ag2CO3 as a raw material. The conditions of CVD can be carried out as follows.

Raw material : Source temperature of Ag2CO3 raw material : 170-degreeC use gas : Ag2CO3/Ar/H2=10/25/1000sccm pressure : 2.6x103Pa substrate heating temperature: By this, the Ag layer 20 deposits on the 450-degreeC insulating layer 12 including the inside of a slot 14. The Ag layer 20 is formed of the following reaction.

Ag2CO3+H2->2Ag+CO2**+H2O** [0052] The CVD system of this invention shown in drawing 3 for formation of the Ag layer 20 was used. This CVD system is equipped with the piping 204 which connects the CVD chamber 200, the source 202 of a raw material, the source of a raw material, and a CVD chamber. And it has the 1st heater 206 which heats piping 204 more than the boiling point of a raw material, and the 2nd heater 210 which heats the CVD chamber induction 208 for introducing a raw material into a CVD chamber more than the boiling point of a raw material. The 2nd heater 210 is lamp heating apparatus, and the mirror 212 is formed. Moreover, the aperture 214 made from a quartz is formed in the part of the about 208 CVD chamber induction [which opposes the 2nd heater 210] piping 204. In addition, it is a heater for lamp heating apparatus for 216 to heat a base 10 and 218 to heat inert gas induction among drawing 3 , and for 220 heat the source 202 of a raw material. At the 1st and 2nd heaters 206,210, Ag2CO3 gas which flows the inside of piping 204 and the CVD chamber induction 208 is held more than 218-degreeC which is the boiling point.

[0053] By [a process -140], next the chemical mechanical polish method, the Ag layer 20 and the adhesion layer 16 on an insulating layer 12 are ground chemically and mechanically, and are removed, in a slot 14, it leaves the Ag layer 20 and the adhesion layer 16, and wiring which consists of the metal wiring layer 22 is formed (refer to drawing 1). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be carried out as follows.

Polish plate rotational frequency : 37rpm substrate maintenance base rotational frequency : 17rpm polishing pressure force : 5.5x108Pa pad temperature : A chemical mechanical polish is performed using the mixed water solution of 40 degreeCI2+KI.

[0054] since a slurry (abrasive material +KOH+ water of SiO2 system) is used when grinding SiO2 conventionally, but it is not distributed at homogeneity in the field which a slurry should grind in case SiO2 is ground by the slurry -- grinding -- passing -- etc. -- the problem that dispersion arises is in flattening of the polished surface in a substrate. When grinding the Ag layer 20 and the adhesion layer 16, a slurry is not needed, but by grinding with the mixed water solution of I2+KI, it is possible to remove only the Ag layer 20 and the adhesion layer 16, and it has the advantage that there is also little dispersion, in flattening of the polished surface in a substrate.

[0055] Wiring which consists of the metal wiring layer 22 embedded at the flat insulating layer 12 by this is formed. In an example 1, like the conventional wiring formation approach, regist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of regist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary.

[0056] (Example 2) In the example 1, the metal wiring layer 22 which consists of the Ag layer 20 and the adhesion layer 16 on an insulating layer 12 was removed by the chemical mechanical polish method. The metal wiring layer 22 is removed [in / instead / an example 2] by the etchback method by dry etching. In addition, other processes are the same as an example 1, and detailed explanation is omitted.

[0057] Etchback is carried out by the dry etching method of the following conditions, and it leaves the metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20 in a slot 14 for the Ag layer 20 and the adhesion layer 16 which were formed on the insulating layer 12 including the [etching process of metal wiring layer 22] slot 14.

Gas used : NO2/O2=20 / 20sccm microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : 100-degreeC [0058] (Example 3) In an example 3, the process which forms the sidewall 26 which changes from SiN to the side attachment wall of a slot 14 between the [process -110] of an example 1 and [a process -120] is included further. In addition, other processes are the same as an example 1, and detailed explanation is omitted. Hereafter, the formation process of the sidewall 26 of an example 3 is explained with reference to drawing 5 . By forming a sidewall 26, oxidation of the adhesion layer 16 by the insulating layer 12 can be prevented.

[0059] SiN layer 26A is made to deposit by the plasma-CVD method the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall 26] slot 14 (refer to (A) of drawing 5). The formation conditions of SiN layer 26A are illustrated below.

Gas used: SiH4/NH3/N2=180/500/720sccm temperature : 200-degreeC pressure : 40Pa thickness : 100nm [0060] Then, whole surface etchback of the SiN layer 26A is carried out (refer to (B) of drawing 5). The conditions of etchback can be carried out as follows.

Gas used : CHF3=50sccmRF power : 300W pressure : 2Pa of sidewalls 26 is formed in the side attachment wall of a slot 14 of this. Henceforth, the wiring structure shown in (C) of drawing 5 can be formed through [process -120] - [a process -140]. [of an example 1]

[0061] (Example 4) The wiring structure of an example 4 typical to drawing 6 which shows a sectional view in part Opening 14A formed in 1st insulating-layer 12A on the base 10 which differ an example 1 and a little and consists of a semi-conductor substrate, It consists of metal wiring layers 22 which consist of the adhesion layer 16 and the Ag layer 20 which were embedded at slot 14B formed in 2nd insulating-layer 12B formed on 1st insulating-layer 12A, and opening 14A and slot 14B. In this case, the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the flank of slot 14B may be formed. Moreover, a lower layer conductor layer (for example, source drain field 36) and the wiring 24 in slot 14B are electrically connected by embedding opening 14A by the metal wiring layer 22.

[0062] The wiring formation approaches of an example 4 differ an example 1 and a little, after they form slot 14B in 2nd insulating-layer 12B formed on 1st insulating-layer 12A in opening 14A again at 1st insulating-layer 12A on the base 10 which consists of a semi-conductor substrate beforehand, embed opening 14A and slot 14B by the metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20, and form wiring structure. The metal wiring layer 22 on

2nd insulating-layer 12B is removed by the chemical mechanical polish method. Hereafter, the wiring formation approach of an example 4 is explained with reference to typical drawing 7 and typical drawing 8 which are sectional views a part, such as a semiconductor device.
[0063] On the base 10 which consists of the semi-conductor substrate which consists of [Process] -400 Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, in order to form the gate sidewall 34 in the whole surface, SiO2 film is made to deposit, after performing a LDD ion implantation. The deposition conditions of SiO2 film can be carried out as follows.
Gas used : SiH4/O2-/N2=250/250 / 100sccm temperature : 420-degreeC pressure : 13.3Pa thickness : Further, whole surface etchback of SiO2 film is performed and 0.25 micrometers of gate sidewalls 34 are formed in the side attachment wall of the gate field 32. Whole surface etchback can be performed on condition that the following.
Gas used : C4F8=50sccmRF power: 1200W pressure : An impurity ion implantation is performed on condition that the following after that [2Pa] for formation of the source drain field 36. formation As of an N type channel Formation BF 2 of 20KeV and 5x1015-/cm2 P type channel 20KeV and 3x1015-/cm2 -- a part typical to (A) of drawing 7 in this way -- the structure shown with a sectional view can be acquired.
[0064] 1st insulating-layer 12A which consists of two-layer [of SiO2 and BPSG] is formed in the whole surface with the CVD method of the following conditions after that [[process -410]]. SiO two-layer formation use gas : TEOS 50sccm pressure : 40Pa temperature : 720-degreeC thickness : Formation use gas of 400nmBPSG layers : SiH4/PH3/B-2H6/O2/N2=80/7/7/1000/32000sccm temperature : 400-degreeC pressure : 1.0x105Pa thickness : 500nm 900 more degreeC and reflow processing for 20 minutes are performed, and flattening of 1st insulating-layer 12A is performed.
[0065] [A process -420], next 2nd insulating-layer 12B which consists of SiO2 are formed in the whole surface. 2nd insulating-layer 12B can be formed on condition that the following.
Gas used : SiH4/O2-/N2=250/250 / 100sccm temperature : 420-degreeC pressure : 13.3Pa thickness : 0.8 micrometers [0066] Slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -110] of an example 1 after that [[process -430]] (refer to (B) of drawing 7).
[0067] [Process -440] Subsequently opening 14A is formed in 1st insulating-layer 12A by performing dry etching after regist patterning (refer to (C) of drawing 7). Here, width of face of slot 14B is made larger than the path of opening 14A. The conditions of dry etching can be carried out as follows.
Gas used : C4F8 50sccmRF power: 1200W pressure : Further, 2Pa of 1100-degreeC and activation annealing for 10 seconds are performed, after forming a junction field by performing an ion implantation to opening circles. The following examples can be given as conditions for an ion implantation.
Formation As of an N type channel Formation BF 2 of 20KeV and 5x1015-/cm2 P type channel 20KeV, 3x1015-/cm2 [0068] It is desirable to form a SiN layer in the whole surface by the plasma-CVD method, to carry out whole surface etchback of the SiN layer subsequently like [the formation process of a sidewall 26] of an example 3, and to form the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the side attachment wall of slot 14B after that [[process -450]], (refer to (A) of drawing 8).
[0069] The adhesion layer 16 which consists of Ti layer / TiN layer is formed in a spatter from under [a process -460] next on 2nd insulating-layer 12B containing opening 14A and slot 14B. This process can be made to be the same as that of the [process -120] of an example 1.
[0070] The Ag layer 20 is formed in the whole surface like the [process -130] of an example 1 after that [[process -470]] by the chemistry gaseous-phase depositing method using Ag2CO3 as a raw material (refer to (B) of drawing 8).
[0071] Like [a process -480], next the [process -140] of an example 1, by the chemical mechanical polish method, the Ag layer 20 and the adhesion layer 16 on 2nd insulating-layer 12B are ground chemically and mechanically, and are removed, in slot 14B and opening 14A, it leaves the Ag layer 20 and the adhesion layer 16, and the connection hole and wiring which consist of

the metal wiring layer 22 are formed (refer to drawing 6). That is, the connection hole (for example, the so-called contact hole) with which the metal wiring layer 22 was embedded is formed in opening 14A. Moreover, the wiring 24 with which the metal wiring layer 22 was embedded at slot 14B is formed.
[0072] In addition, it is also removable by carrying out etchback by the dry etching method like an example 2 instead of removing the metal wiring layer 22 which consists of the Ag layer 20 and the adhesion layer 16 by the chemical mechanical polish method.
[0073] (Example 5) An example 5 is deformation of an example 4. Although the wiring structure of an example 5 is the same as an example 4, the wiring formation approach is different from an example 4. That is, opening 14A prepared in 1st insulating-layer 12A is embedded with the metal wiring material which consists of Ag, connection hole 24A is completed, subsequently to a it top, 2nd insulating-layer 12B is made to deposit, and the point which forms slot 14B in this 2nd insulating-layer 12B is different from an example 4. In an example 5, [the process -400], [a process -410], and [a process -440] of an example 4 are same process, and other processes differ. Hereafter, the approach of an example 5 is explained with reference to drawing 9 and drawing 10 .
[0074]
On the base 10 which consists of the semi-conductor substrate of [process -500] -[process -520] Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for formation of the source drain field 36. Then, 1st insulating-layer 12A which consists of two-layer [of SiO2 and BPSG] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed. Subsequently, activation annealing is performed after making a junction field form by forming opening 14A in 1st insulating-layer 12A in the dry etching after regist patterning, and performing an ion implantation to it at opening circles. These processes can be made to be the same as that of the [process -400] of an example 4, [a process -410], and [a process -440]. Subsequently, the sidewall (not shown) which consists of SiN may be formed in the side attachment wall of opening 14A.
[0075] [Process -530]
1st adhesion layer 16A which consists of Ti/TiN is formed in the whole surface from the bottom after [a process -520] by the same approach as the [process -120] of an example 1. Subsequently, by the same approach as the [process -130] of an example 1, 1st Ag layer 20A is formed on the whole surface with a CVD method, and the 1st metal wiring layer which consists of 1st adhesion layer 16A and 1st Ag layer 20A is formed (refer to (A) of drawing 9).
[0076] After that [[process -540]], the 1st metal wiring layer on 1st insulating-layer 12A is removed by the chemical mechanical polish method, and it leaves the 1st metal wiring layer 20A and 16A only in opening 14A (refer to (B) of drawing 9). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -140] of an example 1. Of this, the so-called contact hole 24A by which the 1st metal wiring layer was embedded at opening 14A is formed. Instead of the chemical mechanical polish method, it may leave the 1st metal wiring layer 20A and 16A only in opening 14A with the etchback by the dry etching method like an example 2.

[0077] [Process -550] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO2 is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -420] of an example 4. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -430] of an example 4 (refer to (A) of drawing 10). Then, if needed, a SiN layer may be formed in the whole surface by the plasma-CVD method, subsequently whole surface etchback of the SiN layer may be carried out like the [process -450] of an example 4, and the sidewall (not shown) which changes from SiN to the side attachment wall of slot 14B by this may be formed.
[0078] By the same approach as [a process -560], next the [process -120] of an example 1 After forming in a spatter 2nd adhesion layer 16B which consists of Ti with a thickness of 30nm on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -130] of

an example 1 2nd Ag layer 20B is formed on the whole surface with a CVD method, and the 2nd metal wiring layer which consists of 2nd adhesion layer 16B and 2nd Ag layer 20B is formed.
[0079] [Process -570] Subsequently, by the chemical mechanical polish method, the 2nd metal wiring layer 20B and 16B on 2nd insulating-layer 12B is removed, in slot 14B, it leaves 2nd Ag layer 20B and 2nd adhesion layer 16B, and wiring 24 is formed (refer to (B) of drawing 10). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -140] of an example 1.
[0080] In addition, instead of removing the 2nd metal wiring layer 20B and 16B on 2nd insulating-layer 12B by the chemical mechanical polish method, like an example 2, etchback of the 2nd metal wiring layer 20B and 16B is carried out by the dry etching method, it can leave the 2nd metal wiring layer 20B and 16B only in slot 14B, and wiring 24 can also be formed in slot 14B by this.
[0081] (Example 6) An example 6 is deformation of an example 5. The point that an example 6 is different from an example 5 is in the point which forms a tungsten plug with a CVD method in opening 14A beforehand. Hereafter, the wiring formation approach of an example 6 is explained with reference to drawing 11 .
[0082]
[Process -600] - [a process -620] These processes can be made to be the same as that of [process -500] - [a process -520]. [of an example 5]
[0083] [Process -630]
The barrier layer 40 which consists of Ti/TiN is formed in the whole surface in a spatter after [a process -620], and the tungsten layer 42 is formed with a CVD method all over after that (refer to (A) of drawing 11). The membrane formation conditions of Ti and TiN can be made to be the same as that of the [process -120] of an example 1. Moreover, the membrane formation conditions of the tungsten by the CVD method are illustrated below.
Gas used : WF6/H2=95 / 550sccm membrane formation temperature : 450-degreeC pressure : 1.1x104Pa thickness : 0.4 micrometers [0084] After that [[process -640]], etchback is performed by the dry etching method, the tungsten layer 42 and the barrier layer 40 on 1st insulating-layer 12A are removed, and it leaves the metal plug and the barrier layer 40 which consist of the tungsten layer 42 only in opening 14A (refer to (B) of drawing 11). The conditions of dry etching can be carried out as follows.
Gas used : SF6=50sccm microwave power: 850WRF power : 150W pressure : Contact hole 24A which consists of the so-called tungsten plug by which the tungsten was embedded at opening 14A by this 1.33Pa is formed. In addition, it may leave the tungsten layer 42 and the barrier layer 40 only in opening 14A by the chemical mechanical polish method instead of the etchback by the dry etching method.
[0085] [Process -650] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO2 is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -550] of an example 5. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -550] of an example 5. In addition, width of face of slot 14B is made larger than the path of opening 14A.
[0086] After forming in a spatter the adhesion layer 16 which consists of Ti of 30nm thickness by the same approach as [a process -660], next the [process -560] of an example 5 on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -130] of an example 1, the Ag layer 20 is formed on the whole surface with a CVD method, and the metal wiring layer which consists of the adhesion layer 16 and the Ag layer 20 is formed.
[0087] The metal wiring layer on 2nd insulating-layer 12B is removed with the etchback by the chemical mechanical polish method or dry etching after that [[process -670]] by the same approach as the [process -140] of an example 1. By this, it leaves a metal wiring layer only in slot 14B, and the wiring 24 which consisted of metal wiring layers which consist of the adhesion layer 16 and the Ag layer 20 in slot 14B is formed (refer to (C) of drawing 11).
[0088] (Example 7) an example 7 - an example 12 -- the 2nd voice of this invention -- the wiring structure of the semiconductor device applied like, and the 2nd voice -- it is related with the wiring formation approach which starts like. The wiring structure of an example 7 changes

from the multilayer metal wiring layer 50 formed in the slot 14 where a semiconductor device is typical, and which was formed in the insulating layer 12 on a base 10, and the slot 14 to drawing 12 so that a sectional view may be shown in part. The metal wiring layer 50 consists of an adhesion layer 52, a Cu layer 54, and an Ag layer 56 from the bottom. Moreover, the adhesion layer 52 is the two-layer structure of Ti layer 52 A/TiN layer 52B from the bottom.
[0089] the wiring formation approach of an example 7 -- (**) -- the process which forms a slot 14 in an insulating layer 12 after forming an insulating layer 12 on a base 10, and (**) -- it consists on an insulating layer 12 including a slot 14 of the process which forms from the bottom the multilayer metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56, and the process which removes the metal wiring layer 50 on an insulating layer (Ha) 12, and leaves a metal wiring layer in a slot 14.
[0090] Formation of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 is performed in a spatter. Moreover, removal of the metal wiring layer 50 on the insulating layer 12 in the process of (Ha) consists of the chemical mechanical polish process of the metal wiring layer 50. By operating as a stopper the insulating layer 12 which consists of SiO2, it becomes possible to set up the selection ratio of the metal wiring layer 50 and insulating layer 12 to a chemical mechanical polish to infinity.
[0091] Hereafter, with reference to typical drawing 13 which is sectional views a part, such as a semiconductor device, the wiring formation approach of an example 7 is explained concretely.
[0092] The insulating layer 12 which consists of SiO2 is formed on the base 10 which consists of [a process -700, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be made to be the same as that of the [process -100] of an example 1. Then, a slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique. In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 13 . The conditions of dry etching can be made to be the same as that of the [process -110] of an example 1.
[0093] The adhesion layer 52 which consists of Ti layer 52 A/TiN layer 52B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -710] next (refer to (A) of drawing 13). The adhesion layer 52 can be made to be the same as that of the [process -120] of an example 1.
[0094] The copper (Cu) layer 54 is formed in the whole surface in a spatter after that [[process -720]] (refer to (B) of drawing 13). The Cu layer 54 can be formed on the following spatter conditions.
Gas used : Ar=100sccm power : 10kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 500nm [0095] The silver (Ag) layer 56 is formed in the whole surface in a spatter after that [[process -730]] (refer to (C) of drawing 13). The Ag layer 56 can be formed in the spatter of the following conditions.
Gas used : Ar=100sccm power : 10kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 100nm of front faces of the Cu layer 54 is covered with the Ag layer 56 in this way.
[0096] By [a process -740], next the chemical mechanical polish method, the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on an insulating layer 12 are ground chemically and mechanically, and are removed, in a slot 14, it leaves the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and wiring which consists of the metal wiring layer 50 is formed (refer to drawing 12). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be carried out as follows.
Polish plate rotational frequency : 37rpm substrate maintenance base rotational frequency : 17rpm polishing pressure force : 5.5x108Pa pad temperature : The mixed water solution of I2+KI is used for removal by the chemical mechanical polish method of the 40-degreeCAg layer 56. Moreover, K4Fe(CN)6+H2O is used for removal by the chemical mechanical polish method of the Cu layer 54 and the adhesion layer 52.
[0097] since a slurry (abrasive material +KOH+ water of SiO2 system) is used when grinding SiO2 conventionally, but it is not distributed at homogeneity in the field which a slurry should grind in case SiO2 is ground by the slurry -- grinding -- passing -- etc. -- the problem that

dispersion arises is in flattening of the polished surface in a substrate. When grinding the Ag layer 56, the Cu layer 54, and the adhesion layer 52, a slurry is not needed, but by grinding in the mixed water solution of I2+KI, and K4Fe(CN)6 water solution, it is possible to remove only the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and it has the advantage that there is also little dispersion, in flattening of the polished surface in a substrate.
[0098] Wiring which consists of the metal wiring layer 50 embedded at the flat insulating layer 12 by this is formed. In an example 7, like the conventional wiring formation approach, regist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of regist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary.
[0099] (Example 8) In the example 7, the metal wiring layer 50 which consists of the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on an insulating layer 12 was removed by the chemical mechanical polish method. The metal wiring layer 50 is removed [in / instead / an example 2] by the etchback method by dry etching. In addition, other processes are the same as an example 7, and detailed explanation is omitted.
[0100] Etchback is carried out by the dry etching method of the following conditions, and it leaves the metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 in a slot 14 for the Ag layer 56, the Cu layer 54, and the adhesion layer 52 which were formed on the insulating layer 12 including the [etching process of metal wiring layer 50] slot 14. The etching use gas of the Ag layer 56 : NO2/O2=20 / 20sccm microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : Etching use gas of the 100-degreeCCu layer 54 and the adhesion layer 52 : O2-/Cl2=10 / 70sccm microwave power: 1000WRF power : 300W pressure : 0.5Pa substrate heating temperature : 300-degreeC [0101] (Example 9) In an example 9, the process which forms the sidewall 26 which changes from SiN to the side attachment wall of a slot 14 between the [process -710] of an example 7 and [a process -720] is included further. In addition, other processes are the same as an example 7, and detailed explanation is omitted. Hereafter, the formation process of the sidewall 26 of an example 9 is explained with reference to drawing 14 . By forming a sidewall 26, oxidation of the adhesion layer 52 by the insulating layer 12 and the Cu layer 54 can be prevented.
[0102] SiN layer 26A is made to deposit by the plasma-CVD method the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall 26] slot 14 (refer to (A) of drawing 14). Next, whole surface etchback of the SiN layer 26A is carried out (refer to (B) of drawing 14). The formation conditions of SiN layer 26A and the conditions of etchback can be made to be the same as that of an example 3. A sidewall 26 is formed in the side attachment wall of a slot 14 of this. Henceforth, the wiring structure shown in (C) of drawing 14 can be formed through [process -720] - [a process -740]. [of an example 7]
[0103] (Example 10) The sidewall 26 which consists of SiN in an example 9 was formed in the side attachment wall of a slot 14. On the other hand, in an example 10, a sidewall is formed from Ag (silver). In addition, other processes are the same as an example 7, and detailed explanation is omitted. Hereafter, the formation process of the sidewall of an example 10 is explained. By forming the sidewall which consists of Ag, oxidation of the adhesion layer 52 by the insulating layer 12 and the Cu layer 54 can be prevented.
[0104] Ag layer is made to deposit in a spatter the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall which consists of Ag] slot 14. Next, whole surface etchback of the Ag layer is carried out. The formation conditions of Ag layer and the conditions of etchback are illustrated below.
Ag stratification condition use gas : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 100nmAg layer etchback condition use gas : NO2/O2=20 / 20sccm microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : 100degreeC -- the same sidewall can be formed in the side attachment wall of a slot 14 with having been shown in drawing 14 in this way. Henceforth, the same wiring structure can be formed with having been shown in (C) of drawing 14 through [process -720] - [a process -740]. [of an example 7]

[0105] (Example 11) The wiring structure of an example 11 typical to drawing 15 which shows a sectional view in part Opening 14A formed in 1st insulating-layer 12A on the base 10 which differ an example 7 and a little and consists of a semi-conductor substrate, It consists of metal wiring layers 50 which consist of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 which were embedded at slot 14B formed in 2nd insulating-layer 12B formed on 1st insulating-layer 12A, and opening 14A and slot 14B. In this case, the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the flank of slot 14B may be formed. Moreover, a lower layer conductor layer (for example, source drain field 36) and the wiring 58 in slot 14B are electrically connected by embedding opening 14A by the metal wiring layer 50.
[0106] The wiring formation approaches of an example 11 differ an example 7 and a little, after they form slot 14B in 2nd insulating-layer 12B formed on 1st insulating-layer 12A in opening 14A again at 1st insulating-layer 12A on the base 10 which consists of a semi-conductor substrate beforehand, embed opening 14A and slot 14B by the metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56, and form wiring structure. The metal wiring layer 50 on 2nd insulating-layer 12B is removed by the chemical mechanical polish method. Hereafter, the wiring formation approach of an example 11 is explained with reference to typical drawing 16 which is sectional views a part, such as a semiconductor device.
[0107] On the base 10 which consists of the semi-conductor substrate of [Process] -1100 Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for source drain field formation.
[0108] After that [[process -1110]], 1st insulating-layer 12A which consists of two-layer [of SiO2 and BPSG] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed.
[0109] [Process -1120] Subsequently to a 1st insulating-layer 12A top, 2nd insulating-layer 12B which consists of SiO2 is formed.
[0110] Slot 14B is formed in 2nd insulating-layer 12B after that [[process -1130]].
[0111] [Process -1140] Opening 14A is further formed in 1st insulating-layer 12A. Subsequently, activation annealing is performed after making a junction field form by performing an ion implantation to opening circles.
[0112] The above process can be made to be the same as that of [process -400] - [a process -440]. [of an example 4]
[0113] [Process -1150] Subsequently the sidewall 26 which consists of SiN may be formed in the side attachment wall of opening 14A and slot 14B like the [process -450] of an example 4. Of the above process, the structure shown in (A) of drawing 16 is formed.
[0114] The adhesion layer 52 which consists of Ti layer / TiN layer is formed in a spatter from under [a process -1160] next on 2nd insulating-layer 12B containing opening 14A and slot 14B. This process can be made to be the same as that of the [process -120] of an example 1.
[0115] The Cu layer 54 is formed in the whole surface in a spatter like the [process -720] of an example 7 after that [[process -1170]]. Subsequently, the Ag layer 56 is formed in the whole surface in a spatter like the [process -730] of an example 7 (refer to (B) of drawing 16).
[0116] After that [[process -1180]], like the [process -740] of an example 7, by the chemical mechanical polish method, the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on 2nd insulating-layer 12B are ground chemically and mechanically, and are removed, in slot 14B and opening 14A, it leaves the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and the connection hole and wiring which consist of the metal wiring layer 50 are formed (refer to drawing 15). That is, connection hole 58A (for example, the so-called contact hole) where the metal wiring layer 50 was embedded is formed in opening 14A. Moreover, the wiring 58 with which the metal wiring layer 50 was embedded at slot 14B is formed.
[0117] In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the metal wiring layer 50 which consists of the Ag layer 56, the Cu layer 54, and the adhesion layer 52 by the chemical mechanical polish method.
[0118] (Example 12) An example 12 is deformation of an example 11. Although the wiring structure of an example 12 is the same as an example 11, the wiring formation approach is

different from an example 11. That is, after embedding opening 14A prepared in 1st insulating-layer 12A with the metal wiring material which consists of Cu and completing connection hole 58A, 2nd insulating-layer 12B is made to deposit on it, and the point which forms slot 14B in this 2nd insulating-layer 12B is different from an example 11. In an example 12, [the process -1100], [a process -1110], and [a process -1140] of an example 11 are same process, and other processes differ. Hereafter, the approach of an example 12 is explained with reference to drawing 17 .

[0119]

On the base 10 which consists of the semi-conductor substrate of [process -1200] -[process -1220] Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for source drain field formation. Then, 1st insulating-layer 12A which consists of two-layer [of SiO2 and BPSG] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed. Subsequently, activation annealing is performed after making a junction field form by forming opening 14A in 1st insulating-layer 12A in the dry etching after regist patterning, and performing an ion implantation to it at opening circles. These processes can be made to be the same as that of the [process -1100] of an example 4, [a process -1110], and [a process -1140]. Subsequently, the sidewall (not shown) which consists of SiN may be formed in the side attachment wall of opening 14A.

[0120] [Process -1230]

1st adhesion layer 52A which consists of Ti/TiN is formed in the whole surface from the bottom after [a process -1220] by the same approach as the [process -710] of an example 7. Subsequently, by the same approach as the [process -720] of an example 7, 1st Cu layer 54A is formed on the whole surface in a spatter, and the 1st metal wiring layer which consists of 1st adhesion layer 52A and 1st Cu layer 54A is formed.

[0121] After that [[process -1240]], the 1st metal wiring layer on 1st insulating-layer 12A is removed by the chemical mechanical polish method, and it leaves the 1st metal wiring layer 54A and 52A only in opening 14A (refer to (A) of drawing 17). The conditions of a chemical mechanical polish can be made to be the same as that of the chemical mechanical polish of Cu layer of the [process -740] of an example 7. Of this, the so-called contact hole 58A by which the 1st metal wiring layer was embedded at opening 14A is formed. Instead of the chemical mechanical polish method, it may leave the 1st metal wiring layer 54A and 52A only in opening 14A with the etchback by the dry etching method like an example 8.

[0122] [Process -1250] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO2 is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -1120] of an example 11. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -1130] of an example 11. Then, subsequently it can form and be easy to form a SiN layer in the whole surface by the plasma-CVD method, to carry out whole surface etchback of the SiN layer, and to have the sidewall (not shown) which consists of SiN in the side attachment wall of slot 14B by this if needed, like the [process -1150] of an example 11.

[0123] By the same approach as [a process -1260], next the [process -710] of an example 7 After forming in a spatter 2nd adhesion layer 52B which consists of Ti with a thickness of 30nm on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -730] of an example 7 The 2nd metal wiring layer which consists of 2nd adhesion layer 52B, 2nd Cu layer 54B, and the Ag layer 56 is formed by forming 2nd Cu layer 54B on the whole surface in a spatter, and forming the Ag layer 56 in a spatter on it further.

[0124] [Process -1270] Subsequently, by the chemical mechanical polish method, the 2nd metal wiring layer 56, 54B, and 52B on 2nd insulating-layer 12B is removed, in slot 14B, it leaves the Ag layer 56, Cu layer of ** 2nd 54B, and 2nd adhesion layer 52B, and wiring 58 is formed (refer to (B) of drawing 18). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -740] of an example 7.

[0125] In addition, instead of removing the 2nd metal wiring layer 56, 54B, and 52B on 2nd

insulating-layer 12B by the chemical mechanical polish method Like an example 8, etchback of the 2nd metal wiring layer 56, 54B, and 52B is carried out by the dry etching method, by this, it can leave the 2nd metal wiring layer 56, 54B, and 52B only in slot 14B, and wiring 58 can also be formed in slot 14B.

[0126] (Example 13) an example 7 - an example 12 -- setting -- the wiring structure of a semiconductor device -- the 2nd voice of this invention -- it formed by the wiring formation approach which starts like. On the other hand, the wiring structure of the semiconductor device in an example 13 - an example 15 is formed by the wiring formation approach concerning the 3rd mode of this invention.

[0127] The process which forms a slot 14 in an insulating layer 12 after the wiring formation approach of the semiconductor device of an example 13 forms an insulating layer 12 on the (b) base 10, The process which forms from the bottom 1st multilayer metal wiring layer 50A which consists of the adhesion layer 52 and the Cu layer 54 on the insulating layer 12 including the (b) slot 14, The process which removes 1st metal wiring layer 50A on an insulating layer 12, and leaves 1st metal wiring layer 50A in a slot 14, (Ha) It consists of the process which forms 2nd metal wiring layer 50B which consists of Ag layer on the (d) insulating layer 12 and 1st metal wiring layer 50A, and the process which removes 2nd metal wiring layer 50B on the (e) insulating layer 12, and leaves 2nd metal wiring layer 50B in a slot 14.

[0128] The adhesion layer 52, the Cu layer 54, and formation at metal wiring layer 50B to the 2nd are performed in a spatter. Moreover, removal of 2nd metal wiring layer 50B on the insulating layer 12 in the process of (e) changes from the chemical mechanical polish process of the metal wiring layer 50 to removal of 1st metal wiring layer 50A on the insulating layer 12 in the process of (Ha), and a list. By operating as a stopper the insulating layer 12 which consists of SiO2, it becomes possible to set up the selection ratio of the 1st [to a chemical mechanical polish], and 2nd metal wiring layers 50A and 50B, and an insulating layer 12 to infinity.

[0129] In the wiring formation approach concerning the 3rd mode of this invention, the Cu layer 54 can be covered with 2nd metal wiring layer 50B which consists of Ag layer much more more certainly than the wiring formation approach concerning the 2nd mode of this invention.

[0130] Hereafter, with reference to typical drawing 18 and typical drawing 19 which are sectional views a part, such as a semiconductor device, the wiring formation approach of an example 13 is explained concretely.

[0131] The insulating layer 12 which consists of SiO2 is formed on the base 10 which consists of [a process -1300, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be made to be the same as that of the [process -100] of an example 1. Then, a slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique. In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 18 . The conditions of dry etching can be made to be the same as that of the [process -110] of an example 1.

[0132] The adhesion layer 52 which consists of Ti layer 52 A/TiN layer 52B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -1310] next. The adhesion layer 52 can be made to be the same as that of the [process -120] of an example 1.

[0133] The copper (Cu) layer 54 is formed in the whole surface in a spatter after that [[process -1320]] (refer to (A) of drawing 18). Formation of the Cu layer 54 can be made to be the same as that of the [process -720] of an example 7. In this way, 1st multilayer metal wiring layer 50A which consists of the adhesion layer 52 and the Cu layer 54 can be formed from the bottom on the insulating layer 12 including a slot 14.

[0134] By [a process -1330], next the chemical mechanical polish method, the Cu layer 54 and the adhesion layer 52 on an insulating layer 12 are ground chemically and mechanically, and are removed, and it leaves 1st metal wiring layer 50A which consists of the Cu layer 54 and the adhesion layer 52 in a slot 14 (refer to (B) of drawing 18). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be made to be the same as that of an example 13. K4Fe(CN)6+H2O is used for removal by the chemical mechanical polish method of the Cu layer 54 and the adhesion layer 52.

[0135] 2nd metal wiring layer 50B which consists of a silver (Ag) layer is formed in the whole

surface in a spatter after that [[process -1340]] (refer to (A) of drawing 19). Formation of Ag layer can be made to be the same as that of the [process -730] of an example 13. In this way, the front face of 1st metal wiring layer 50A is covered with 2nd metal wiring layer 50B which consists of Ag layer.

[0136] By [a process -1350], next the chemical mechanical polish method, 2nd metal wiring layer 50B which consists of Ag layer on an insulating layer 12 is ground chemically and mechanically, and is removed, it leaves 2nd metal wiring layer 50B which consists of Ag layer in a slot 14, and wiring which consists of the 1st and 2nd metal wiring layers 50A and 50B is formed (refer to (B) of drawing 19). The conditions of a chemical mechanical polish can be made to be the same as that of an example 13. In addition, the mixed water solution of I2+KI is used for removal by the chemical mechanical polish method of Ag layer.

[0137] In an example 13, like the conventional wiring formation approach, regist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of regist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary. Moreover, since the front face of 1st metal wiring layer 50A is covered with 2nd metal wiring layer 50B much more certainly, oxidation of the Cu layer 54 which constitutes 1st metal wiring layer 50A can be prevented.

[0138] In an example 13, although 1st metal wiring layer 50A and 2nd metal wiring layer 50B were chiefly removed by the chemical mechanical polish method, it is also removable like an example 8 with the etchback by the dry etching method.

[0139] Moreover, formation of the sidewall explained in the wiring formation approach, and the example 9 or example 10 of the semiconductor device concerning the 3rd mode of this invention explained in the example 13 is also combinable. Furthermore, the wiring formation approach explained in the example 13 is also applicable instead of the Ag layer 56 in an example 11 or an example 12.

[0140] (Example 14) Only the flow of the process in the case of applying the wiring formation approach explained in the example 13 instead of the Ag layer 56 in an example 11 is explained below. In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the 1st and/or 2nd metal wiring layer by the chemical mechanical polish method.

[0141] Formation of the component isolation region to a [process -1400] base top, and a gate field. LDD ion implantation. Formation of a gate sidewall. The impurity ion implantation for source drain field formation.

[Process -1410] Formation and reflow processing of the 1st of an insulating layer which consist of two-layer [of SiO2 and BPSG].

[Process -1420] Formation of the 2nd insulating layer which consists of SiO2 to a 1st insulating-layer top.

Formation of the slot to the 2nd insulating layer of [a process -1430].

Formation of opening to the 1st insulating layer of [a process -1440].

Formation by the spatter to a 2nd insulating-layer top including opening and the slot of an adhesion layer which consist of a [process -1450] Ti layer / TiN layer.

Formation of Cu layer by the spatter to a [process -1460] adhesion layer top.

Removal of Cu layer on the 2nd insulating layer by the [process -1470] chemical mechanical polish.

Formation of the 2nd metal wiring layer which changes from Ag layer by the spatter to the whole [process -1470] surface.

Removal of the 2nd metal wiring layer on the 2nd insulating layer by the [process -1480] chemical mechanical polish method.

[0142] (Example 15) Only the flow of the process in the case of applying the wiring formation approach explained in the example 13 instead of the Ag layer 56 in an example 12 is explained below. In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the 1st and/or 2nd metal wiring layer by the chemical mechanical polish method.

[0143] Formation of the component isolation region to a [process -1500] base top, and a gate field. LDD ion implantation. Formation of a gate sidewall. The impurity ion implantation for source drain field formation.
[Process -1510] Formation and reflow processing of the 1st of an insulating layer which consist of two-layer [of SiO2 and BPSG].
Formation of opening to the 1st insulating layer of [a process -1520].
[Process -1530] Formation by the spatter of the 1st metal wiring layer which consists of the 1st adhesion layer to a 1st insulating-layer top, and 1st Cu layer.
Removal of the 1st metal wiring layer on the 1st insulating layer by the [process -1540] chemical mechanical polish method. By this, the so-called contact hole where the 1st metal wiring layer was embedded at opening is formed.
Formation of the 2nd insulating layer which consists of SiO2 all over [a process -1550].
Formation of the slot to the 2nd insulating layer.
[Process -1560] Formation by the spatter of the 2nd adhesion layer to a 2nd insulating-layer top, and Cu layer.
Removal of Cu layer on the 2nd insulating layer by the [process -1570] chemical mechanical polish, and the 2nd adhesion layer.
Formation of the 2nd metal wiring layer which changes from Ag layer by the spatter to the whole [process -1580] surface.
Removal of the 2nd metal wiring layer on the 2nd insulating layer by the [process -1590] chemical mechanical polish method.
[0144] As mentioned above, although this invention was explained based on the desirable example, this invention is not limited to these examples. The various ingredients and the conditions of having used in the example are instantiation, and can be changed suitably. Depending on the case, opening can be formed instead of Slots 14 and 14B.
[0145] Although the insulating layer was explained as what consists of the combination of SiO2 or SiO2, and BPSG chiefly, it can constitute from what carried out the laminating of well-known insulating materials, such as BPSG, PSG and BSG, AsSG, PbSG, SbSG, SOG, SiON, or SiN, or these insulating layers to instead of [these].
[0146] In an example 1 - an example 6, although formation of the Ag layer 20 was performed by the chemistry gaseous-phase depositing method for having used Ag2CO3 as a raw material instead, it can be performed by the chemistry gaseous-phase depositing method using AgNO2, AgBr, or AgI as a raw material. The CVD conditions in these cases and the heating conditions of the material gas which flows the inside of piping 204 and the CVD chamber induction 208 at the 1st and 2nd heaters 206,210 in the CVD system shown in drawing 3 are illustrated and combined with below, and a reaction formula is shown.
[0147] raw material: -- source temperature of AgNO2 raw material 450-degreeC gas heating condition: -- more than 140-degreeC -- reaction-formula : 2AgNO2+7H2->2Ag+2NH3**+4H2O** : 150-degreeC use gas : AgNO2/Ar/H2=10/25/1000sccm pressure : 2.6x103Pa substrate heating temperature : [0148] Raw material: Source temperature of an AgBr raw material : 450-degreeC use gas : AgBr/Ar/H2=10/75 / 1000sccm pressure : 2.6x103Pa substrate heating temperature: 500-degreeC gas heating conditions: It is power more than 434-degreeC. : 500W (plasma CVD)
Reaction formula : 2AgBr+H2->2Ag+2HBr** [0149] Raw material: Source temperature of an AgI raw material : 560-degreeC use gas : AgI/Ar/H2=10/100 / 1000sccm pressure : 2.6x103Pa substrate heating temperature: 600-degreeC gas heating conditions: It is power more than 552-degreeC. : 500W (plasma CVD)
Reaction formula : 2AgI+H2->2Ag+2HI** [0150] In an example 7 - an example 15, it can form with a CVD method instead of forming Cu layer and/or Ag layer in a spatter. The formation conditions of Cu layer by the CVD method are illustrated below.
Gas used : Cu (HFA)2/H2=10 / 1000sccm pressure : 2.6x103Pa substrate heating temperature: 350-degreeC power : It is the abbreviation for hexafluoro acetylacetonate in 500W, in addition HFA.
[0151] An adhesion layer can also consist of a Ti layer or a TiN layer instead of Ti layer / TiN

layer. The formation conditions of the Ti layer or the TiN layer in this case can be made to be the same as that of the formation conditions of Ti layer 18A explained at the [process -120] of an example 1, and TiN layer 18B. Or an adhesion layer can also be made into the two-layer structure of Ag layer / Ti layer from the bottom again. In this case, Ag layer can be formed in the spatter of the following conditions. Moreover, the formation conditions of Ti layer can be made to be the same as that of the formation conditions of Ti layer 18A explained at the [process -120] of an example 1.
Spatter condition use gas of Ag layer : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 50nm [0152] TiON and TiW can also be used instead of TiN which constitutes an adhesion layer. Moreover, by the case, the sequence of formation of a slot, formation of a sidewall, and formation of an adhesion layer can be changed, and it can also consider as the order of formation of a slot, formation of an adhesion layer, and formation of a sidewall. Moreover, the metal layer or metallic-compounds layer which constitutes adhesion layers, such as Ti and TiN, can be formed by the forming-membranes methods, such as CVD.
[0153] The silicon layer formed on the various substrates for producing the various component sections, such as an insulating layer in which the MgO substrate, the GaAs substrate, superconducting transistor substrate, and lower layer wiring layer other than a silicon semi-conductor substrate or the semi-conductor substrate with which the source drain field was formed were formed as a base, and a gate electrode which needs to form a connection hole (a contact hole, a beer hall, through hole), and needs to form electrical installation, and a thin film transistor can be mentioned.
[0154] In an example 6, although the tungsten plug was formed in opening 14A using the so-called blanket tungsten CVD method, a tungsten plug may be instead formed in opening 14A with the so-called tungsten selection CVD method. The conditions in this case can be carried out as follows. Gas used : WF6/SiH4/H2/Ar=10/7/1000/10 sccm ** Whenever : 260-degreeC ** Force : 26Pa [0155] This invention is applicable to other semiconductor devices other than an MOS semiconductor device (for example, a bipolar transistor, CCD).
[0156] Various kinds of sputtering systems, such as a magnetron sputtering system, DC sputtering system, RF sputtering system, an ECR sputtering system, and a bias sputtering system that impresses substrate bias, can perform a spatter.
[0157] In the wiring structure concerning the 1st mode of this invention under Ag layer again the 2nd voice of this invention -- the wiring structure which starts like -- setting -- the bottom of Cu layer -- or -- again -- the wiring layer or connection hole under an adhesion layer -- refractory metals, such as Mo and Ti, -- Or a monolayer or various combination ******** can be formed for the silicide of TiW, ZrN, W, WC, TiC, other MoSi2 and WSi2, and TiSi2 grade etc.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is typical drawing of the wiring structure of the semiconductor device of an example 1.
[Drawing 2] typical [semiconductor device / for explaining each process of the wiring formation approach of an example 1] -- it is a sectional view a part.
[Drawing 3] It is the mimetic diagram of the CVD system of this invention.
[Drawing 4] It is the mimetic diagram of the polish equipment suitable for operation of this invention.
[Drawing 5] typical [semiconductor device / for explaining the sidewall formation process of an example 3] -- it is a sectional view a part.
[Drawing 6] It is typical drawing of the wiring structure of the semiconductor device of an example 4.
[Drawing 7] typical [semiconductor device / for explaining each process of the wiring formation approach of an example 4] -- it is a sectional view a part.
[Drawing 8] typical [semiconductor device / for continuing at drawing 7 and explaining each process of the wiring formation approach of an example 4] -- it is a sectional view a part.
[Drawing 9] typical [semiconductor device / for explaining the process of the wiring formation approach of an example 5] -- it is a sectional view a part.
[Drawing 10] typical [semiconductor device / for continuing at drawing 9 and explaining the process of the wiring formation approach of an example 5] -- it is a sectional view a part.
[Drawing 11] typical [semiconductor device / for explaining the process of the wiring formation approach of an example 6] -- it is a sectional view a part.
[Drawing 12] It is typical drawing of the wiring structure of the semiconductor device of an example 7.
[Drawing 13] typical [semiconductor device / for explaining each process of the wiring formation approach of an example 7] -- it is a sectional view a part.
[Drawing 14] typical [semiconductor device / for explaining the sidewall formation process of an example 9] -- it is a sectional view a part.
[Drawing 15] It is typical drawing of the wiring structure of the semiconductor device of an example 11.
[Drawing 16] typical [semiconductor device / for explaining each process of the wiring formation approach of an example 11] -- it is a sectional view a part.
[Drawing 17] typical [semiconductor device / for explaining each process of the wiring formation approach of an example 12] -- it is a sectional view a part.
[Drawing 18] typical [semiconductor device / for explaining each process of the wiring formation approach of an example 13] -- it is a sectional view a part.
[Drawing 19] typical [semiconductor device / for continuing at drawing 18 and explaining each process of the wiring formation approach of an example 13] -- it is a sectional view a part.
[Drawing 20] typical [semiconductor device / for explaining each process in the example of a manufacture process of the conventional semiconductor device] -- it is a sectional view a part.
[Drawing 21] typical [semiconductor device / for explaining each process in the example of a

manufacture process of the conventional semiconductor device following on drawing 20] -- it is a sectional view a part.
[Drawing 22] typical [semiconductor device / for explaining each process in another example of the manufacture process of the conventional semiconductor device] -- it is a sectional view a part.
[Drawing 23] It is drawing for explaining the trouble in the manufacture process of the conventional semiconductor device.
[Description of Notations]
10 Base
12, 12A, 12B Insulating layer
14 14B Slot
14A Opening
16, 16A, 16B Adhesion layer
18A Ti layer
18B TiN layer
20 Ag Layer
22 Metal Wiring Layer
24 Wiring
24A Connection hole
26A SiN layer
26 Sidewall
30 Component Isolation Region
32 Gate Field
34 Gate Sidewall
36 Source Drain Field
40 Barrier Layer
42 Tungsten Layer
50 Metal Wiring Layer
50A The 1st metal wiring layer
50B The 2nd metal wiring layer
52, 52A, 52B Adhesion layer
54, 54A, 54B Cu layer
56 Ag Layer
58 Wiring
58A Connection hole
200 CVD Chamber
202 Source of Raw Material
204 Piping
206 1st Heater
208 CVD Chamber Induction
210 2nd Heater
214 Aperture
216 Lamp Heating Apparatus
218 Inert Gas Induction

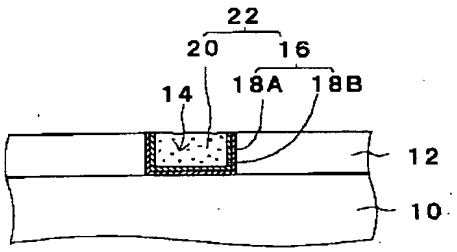
[Translation done.]

* NOTICES *

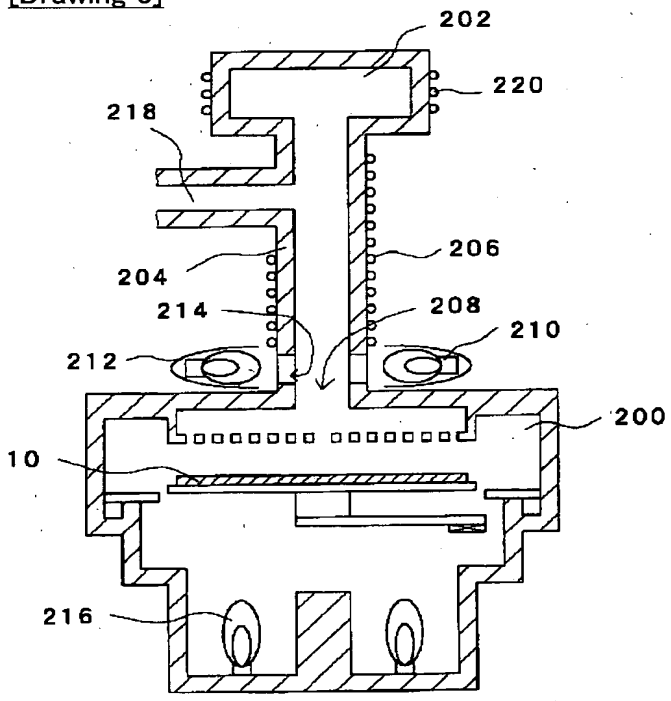
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]
（実施例１の配線構造）

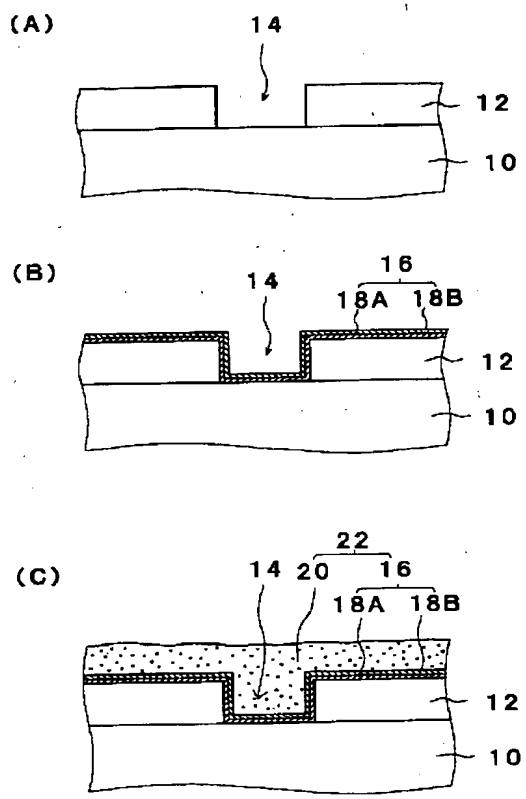


[Drawing 3]

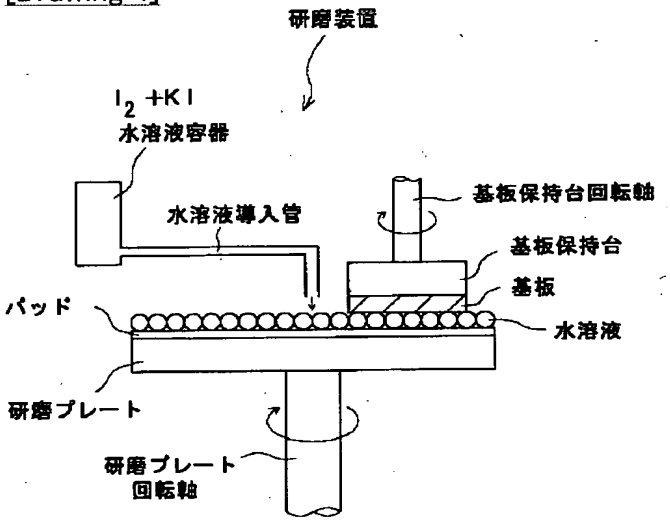


[Drawing 2]

（実施例１の配線形成方法）



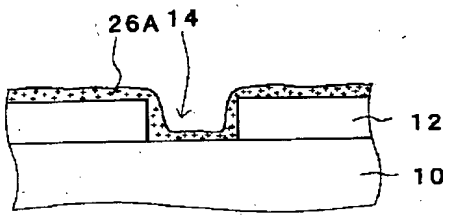
[Drawing 4]



[Drawing 5]

（実施例３の配線形成方法）

(A)



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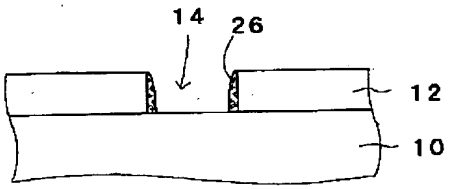

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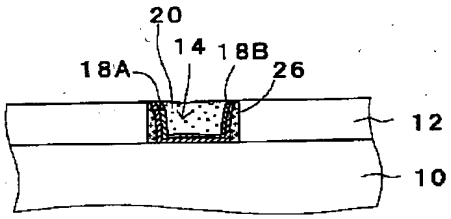
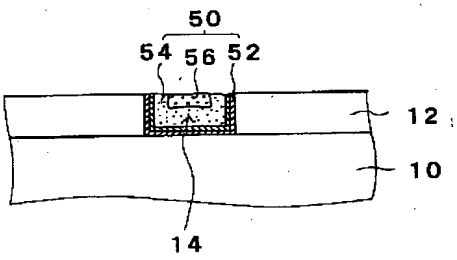


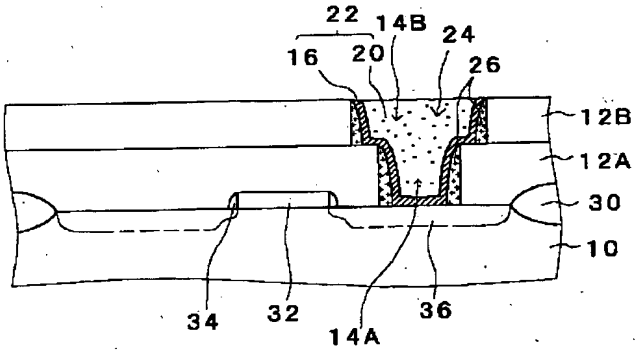
[Drawing 12]

（実施例７の配線構造）



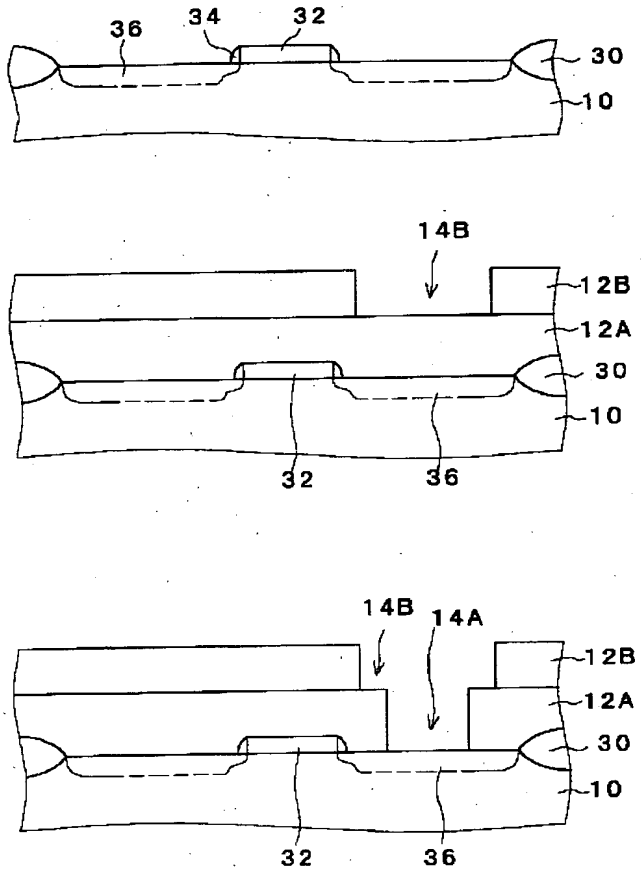
[Drawing 6]

（実施例４の配線構造）



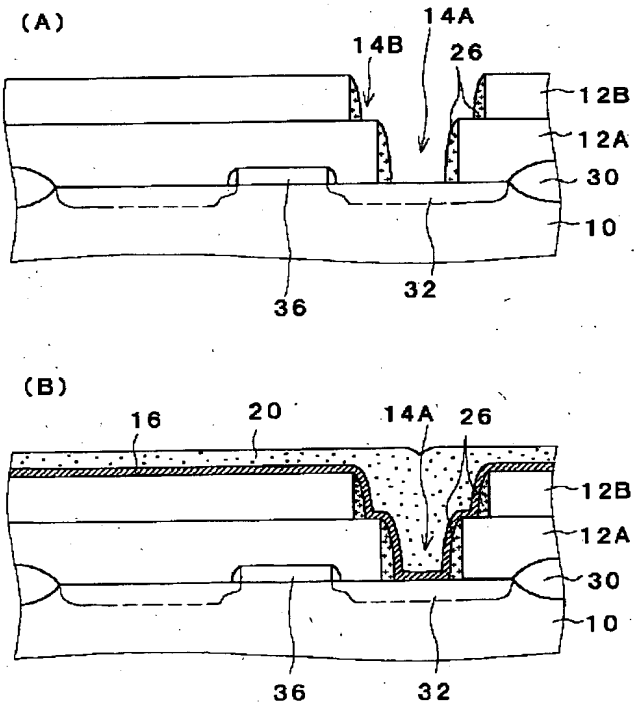
[Drawing 7]

（実施例４の配線形成方法）

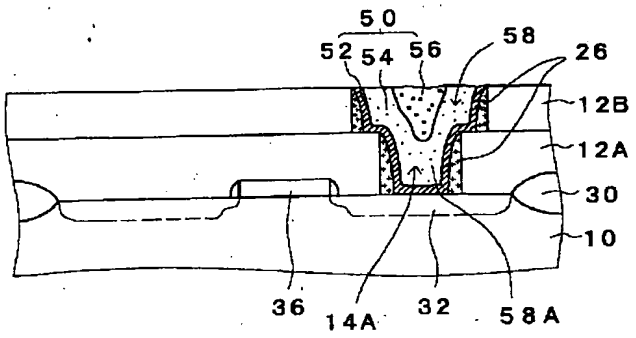


[Drawing 8]

（実施例４の配線形成方法）（続き）

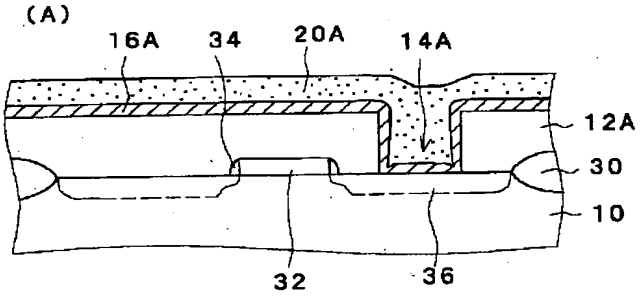


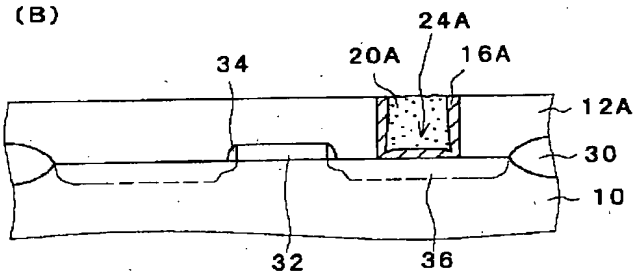
[Drawing 15]



[Drawing 9]

(実施例５の配線形成方法)

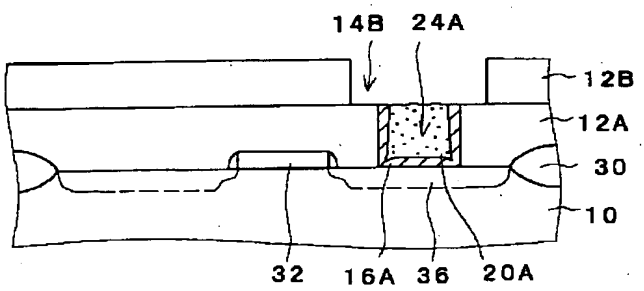




[Drawing 10]

(実施例５の配線形成方法)　(続き)

(A)



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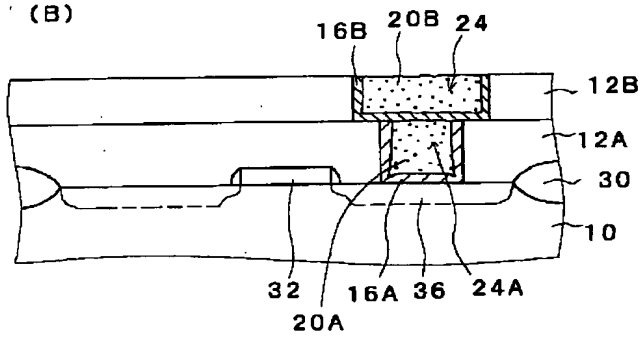
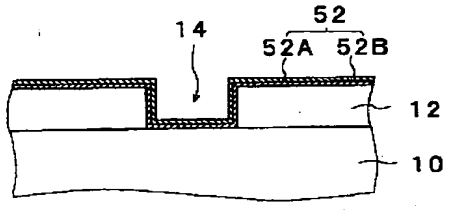


[Drawing 13]

(実施例７の配線形成方法)

(A)



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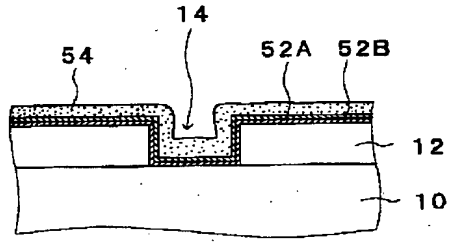

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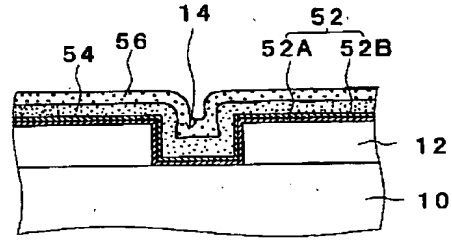
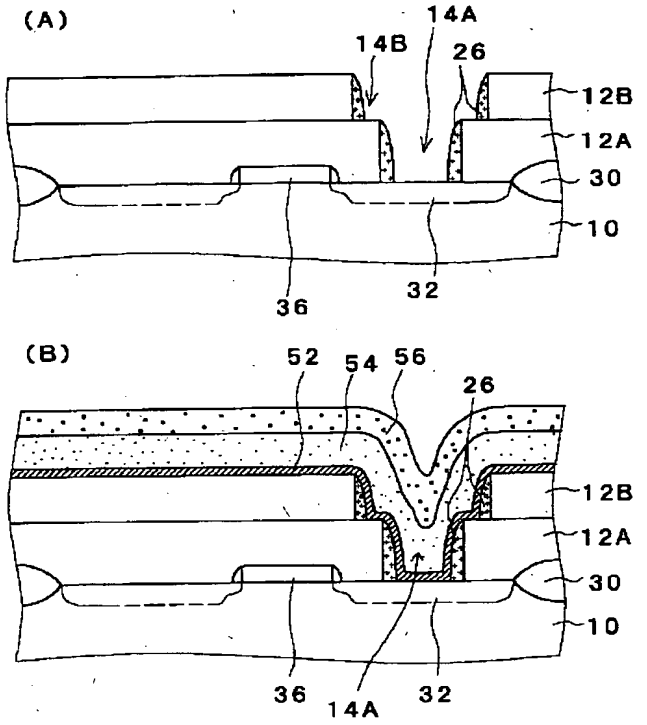


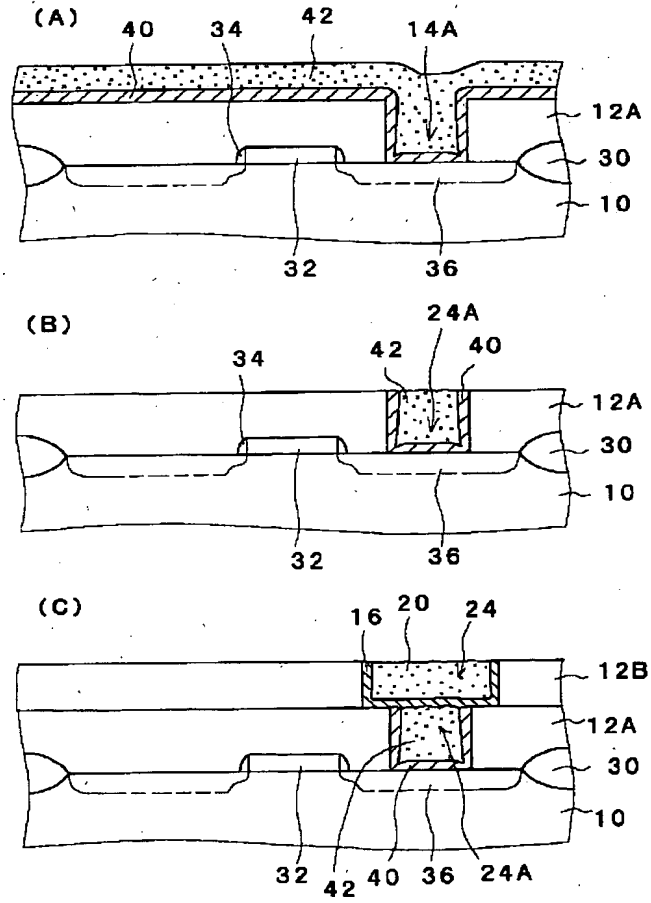
[Drawing 16]

（実施例１１の配線形成方法）



[Drawing 11]

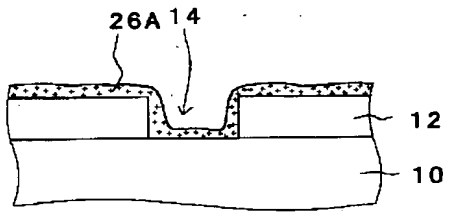
（実施例６の配線形成方法）



[Drawing 14]

（実施例９の配線形成方法）

(A)



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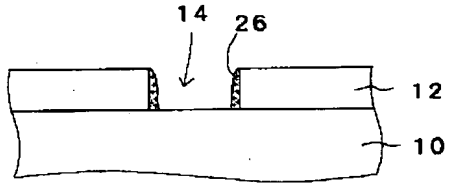

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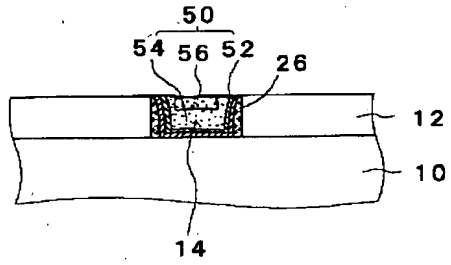
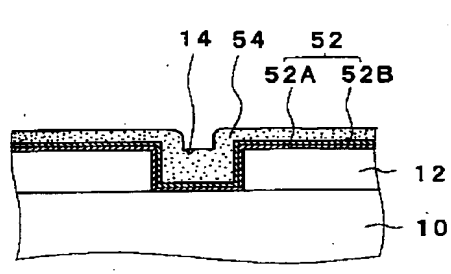


[Drawing 18]

（実施例１３の配線形成方法）

(A)



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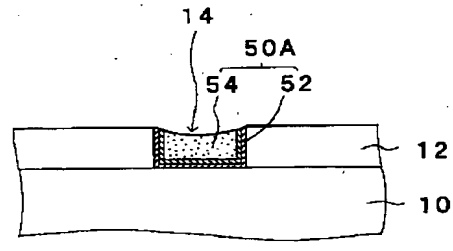
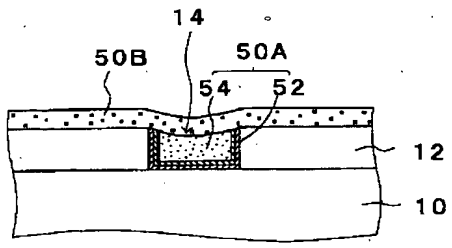


[Drawing 19]

（実施例１３の配線形成方法）　（続き）

(A)



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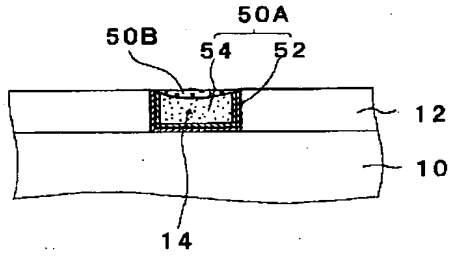
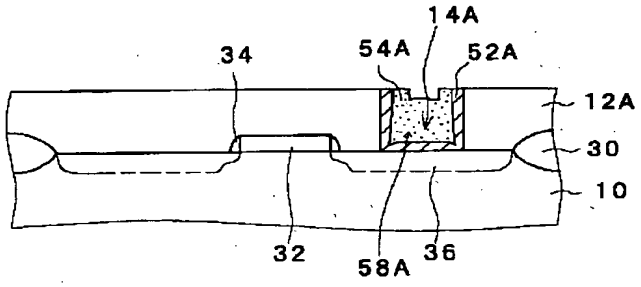


[Drawing 17]

（実施例１２の配線形成方法）

(A)



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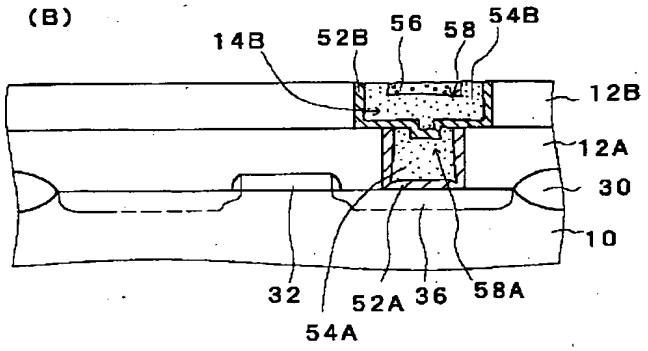
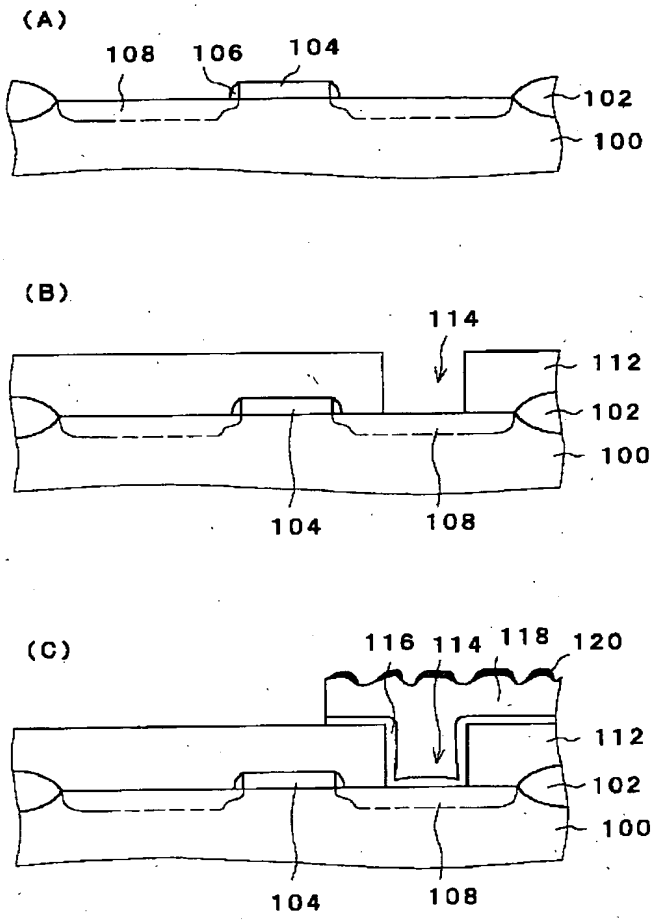


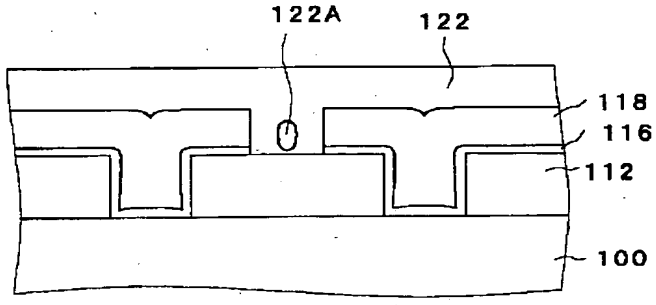
[Drawing 20]

（従来技術，その１）



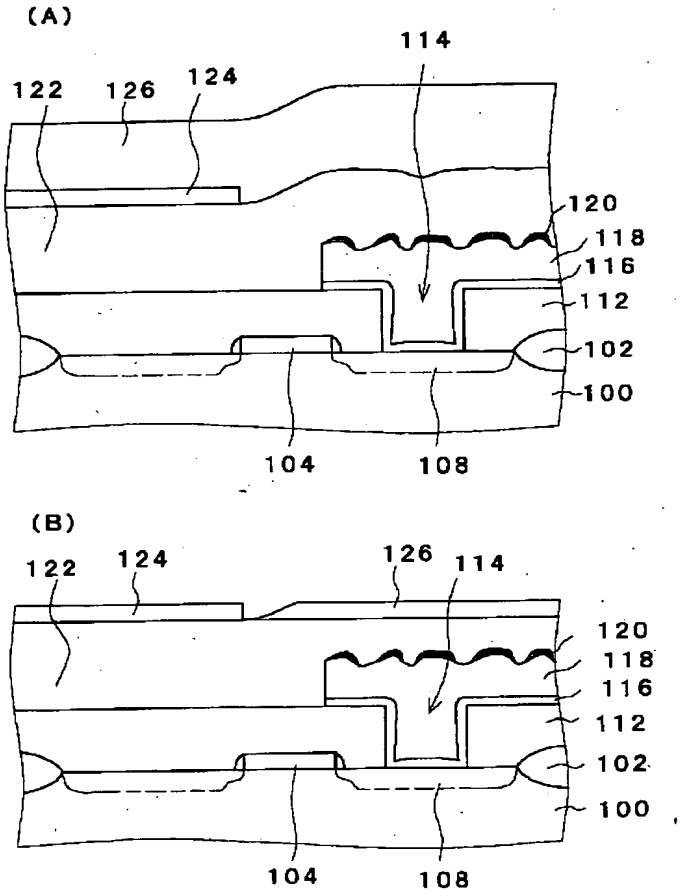
[Drawing 23]

（従来技術における問題点）



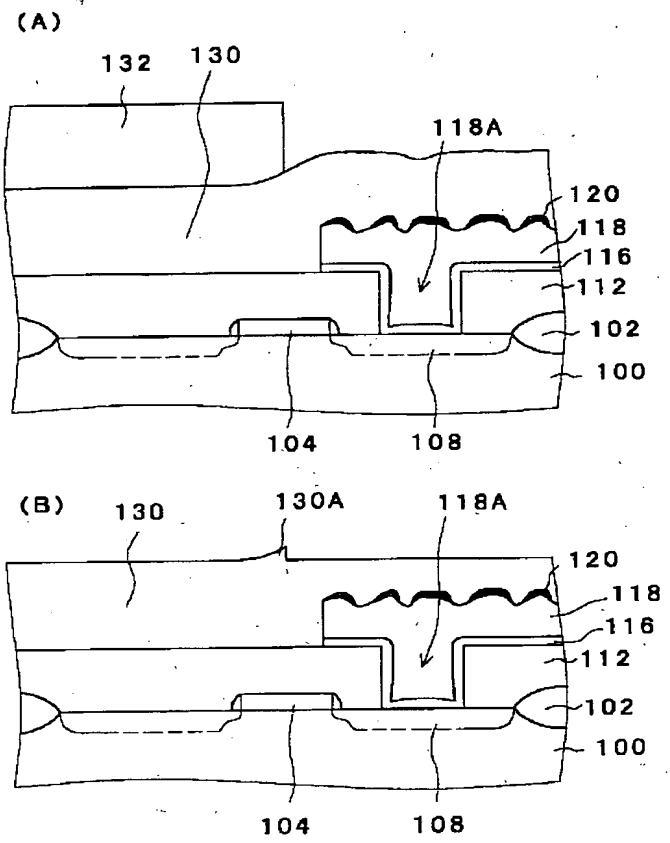
[Drawing 21]

（従来技術，その1）　（続き）



[Drawing 22]

（従来技術，その２）



[Translation done.]

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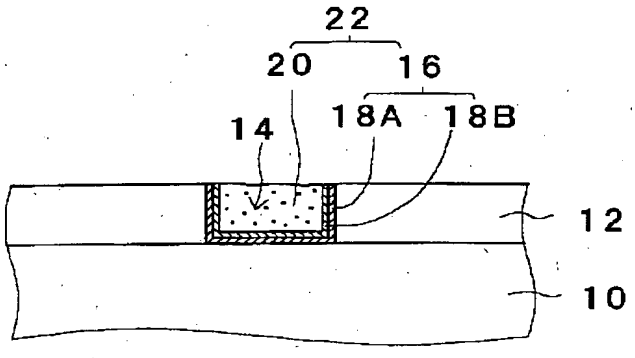
(54)【発明の名称】　半導体装置の配線構造、配線形成方法、銀薄膜形成方法、ＣＶＤ装置並びにケミカルメカニカルポリッシュ法

(57)【要約】

【目的】配線を形成するためのパターニング工程を行う必要がなく、しかも、Ａｌ系合金やＣｕを配線材料として用いた場合の問題点を解決できる、新規の半導体装置の配線構造及び配線形成方法を提供する。

【構成】半導体装置の配線構造は、（イ）基体１０上の絶縁層１２に形成された溝部１４又は開口部と、（ロ）溝部１４又は開口部内に形成された、下から密着１６層及びＡｇ層２０から成る多層２２の金属配線層、から構成されている。半導体装置の配線形成方法は、（イ）基体１０上に絶縁層１２を形成した後、絶縁層１２に溝部１４又は開口部を形成し、（ロ）溝部１４又は開口部内を含む絶縁層上に、下から密着層１６及びＡｇ層２０から成る多層の金属配線層２２を形成し、（ハ）絶縁層１２上の金属配線層２２を除去し、溝部１４又は開口部内に金属配線層２２を残す工程から成る。

（実施例１の配線構造）



【特許請求の範囲】

【請求項１】（イ）基体上の絶縁層に形成された溝部又は開口部と、

（ロ）該溝部又は開口部内に形成された、下から密着層及びＡｇ層から成る多層の金属配線層、

から構成されていることを特徴とする半導体装置の配線構造。

【請求項２】前記密着層は、Ｔｉ層、ＴｉＮ層、下からＴｉ層／ＴｉＮ層の２層構造、若しくは下からＡｇ層／Ｔｉ層の２層構造から成ることを特徴とする請求項１に記載の半導体装置の配線構造。

【請求項３】前記溝部又は開口部の側壁に、ＳｉＮから成るサイドウオールが形成されていることを特徴とする請求項１又は請求項２に記載の半導体装置の配線構造。

【請求項４】（イ）基体上に絶縁層を形成した後、該絶縁層に溝部又は開口部を形成する工程と、

（ロ）該溝部又は開口部内を含む絶縁層上に、下から密着層及びＡｇ層から成る多層の金属配線層を形成する工程と、

（ハ）絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残す工程、

から成ることを特徴とする半導体装置の配線形成方法。

【請求項５】前記Ａｇ層の形成は、Ag_2CO_3、ＡｇＮO_2、ＡｇＢｒ若しくはＡｇＩを原料として用いた化学気相析出法によることを特徴とする請求項４に記載の半導体装置の配線形成方法。

【請求項６】前記（ハ）の工程における絶縁層上の金属配線層の除去は、金属配線層のケミカルメカニカルポリッシュ工程から成ることを特徴とする請求項４又は請求項５に記載の半導体装置の配線形成方法。

【請求項７】I_2とＫＩの混合水溶液を用いてＡｇ層のケミカルメカニカルポリッシュを行うことを特徴とする請求項６に記載の半導体装置の配線形成方法。

【請求項８】前記（ハ）の工程における絶縁層上の金属配線層の除去は、金属配線層のエッチバック工程から成ることを特徴とする請求項４又は請求項５に記載の半導体装置の配線形成方法。

【請求項９】前記密着層は、Ｔｉ層、ＴｉＮ層、下からＴｉ層／ＴｉＮ層の２層構造、若しくは下からＡｇ層／Ｔｉ層の２層構造から成ることを特徴とする請求項４乃至請求項８のいずれか１項に記載の半導体装置の配線形成方法。

【請求項１０】前記（イ）の工程の後に、溝部又は開口部の側壁にＳｉＮから成るサイドウオールを形成する工程を更に含むことを特徴とする請求項４乃至請求項９のいずれか１項に記載の半導体装置の配線形成方法。

【請求項１１】（イ）基体上の絶縁層に形成された溝部又は開口部と、

（ロ）該溝部又は開口部内に形成された、下から密着層、Ｃｕ層及びＡｇ層から成る多層の金属配線層、

から構成されていることを特徴とする半導体装置の配線構造。

【請求項１２】前記密着層は、Ｔｉ層、ＴｉＮ層、下からＴｉ層／ＴｉＮ層の２層構造、若しくは下からＡｇ層／Ｔｉ層の２層構造から成ることを特徴とする請求項１１に記載の半導体装置の配線構造。

【請求項１３】前記溝部又は開口部の側壁には、ＳｉＮから成るサイドウオールが形成されていることを特徴とする請求項１１又は請求項１２に記載の半導体装置の配線構造。

【請求項１４】前記溝部又は開口部の側壁には、Ａｇから成るサイドウオールが形成されていることを特徴とする請求項１１又は請求項１２に記載の半導体装置の配線構造。

【請求項１５】（イ）基体上に絶縁層を形成した後、該絶縁層に溝部又は開口部を形成する工程と、

（ロ）該溝部又は開口部内を含む絶縁層上に、下から密着層、Ｃｕ層及びＡｇ層から成る多層の金属配線層を形成する工程と、

（ハ）絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残す工程、

から成ることを特徴とする半導体装置の配線形成方法。

【請求項１６】前記（ハ）の工程における絶縁層上の金属配線層の除去は、金属配線層のケミカルメカニカルポリッシュ工程から成ることを特徴とする請求項１５に記載の半導体装置の配線形成方法。

【請求項１７】I_2とＫＩの混合水溶液を用いてＡｇ層のケミカルメカニカルポリッシュを行うことを特徴とする請求項１６に記載の半導体装置の配線形成方法。

【請求項１８】前記（ハ）の工程における絶縁層上の金属配線層の除去は、金属配線層のエッチバック工程から成ることを特徴とする請求項１５に記載の半導体装置の配線形成方法。

【請求項１９】（イ）基体上に絶縁層を形成した後、該絶縁層に溝部又は開口部を形成する工程と、

（ロ）該溝部又は開口部内を含む絶縁層上に、下から密着層及びＣｕ層から成る多層の第１の金属配線層を形成する工程と、

（ハ）絶縁層上の第１の金属配線層を除去し、溝部又は開口部内に第１の金属配線層を残す工程と、

（ニ）絶縁層上及び第１の金属配線層上に、Ａｇ層から成る第２の金属配線層を形成する工程と、

（ホ）絶縁層上の第２の金属配線層を除去し、溝部又は開口部内に第２の金属配線層を残す工程、

から成ることを特徴とする半導体装置の配線形成方法。

【請求項２０】前記（ハ）の工程における絶縁層上の第１の金属配線層の除去、又は、前記（ホ）の工程における絶縁層上の第２の金属配線層の除去は、ケミカルメカニカルポリッシュ工程から成ることを特徴とする請求項１９に記載の半導体装置の配線形成方法。

【請求項２１】I_2とＫＩの混合水溶液を用いてＡｇ層のケミカルメカニカルポリッシュを行うことを特徴とする請求項２０に記載の半導体装置の配線形成方法。
【請求項２２】前記（ハ）の工程における絶縁層上の第１の金属配線層の除去、又は、前記（ホ）の工程における絶縁層上の第２の金属配線層の除去は、エッチバック工程から成ることを特徴とする請求項１９に記載の半導体装置の配線形成方法。
【請求項２３】前記密着層は、Ｔｉ層、ＴｉＮ層、下からＴｉ層／ＴｉＮ層の２層構造、若しくは下からＡｇ層／Ｔｉ層の２層構造から成ることを特徴とする請求項１５乃至請求項２２のいずれか１項に記載の半導体装置の配線形成方法。
【請求項２４】前記（イ）の工程の後に、溝部又は開口部の側壁にＳｉＮから成るサイドウオールを形成する工程を更に含むことを特徴とする請求項１５乃至請求項２３のいずれか１項に記載の半導体装置の配線形成方法。
【請求項２５】前記（イ）の工程の後に、溝部又は開口部の側壁にＡｇから成るサイドウオールを形成する工程を更に含むことを特徴とする請求項１５乃至請求項２３のいずれか１項に記載の半導体装置の配線形成方法。
【請求項２６】Ag_2CO_3を原料として用いた化学気相析出法による銀薄膜の形成方法。
【請求項２７】$AgNO_2$を原料として用いた化学気相析出法による銀薄膜の形成方法。
【請求項２８】ＡｇＢｒを原料として用いた化学気相析出法による銀薄膜の形成方法。
【請求項２９】ＡｇＩを原料として用いた化学気相析出法による銀薄膜の形成方法。
【請求項３０】原料源と、ＣＶＤチャンバと、原料源とＣＶＤチャンバとを結ぶ配管とを備えたＣＶＤ装置であって、配管を原料の沸点以上に加熱する第１のヒーターと、原料をＣＶＤチャンバに導入するためのＣＶＤチャンバ導入部を原料の沸点以上に加熱する第２のヒーターとを備えていることを特徴とするＣＶＤ装置。
【請求項３１】第２のヒーターはランプ加熱装置であることを特徴とする請求項３０に記載のＣＶＤ装置。
【請求項３２】I_2及びＫＩの混合水溶液を用いて銀薄膜を化学的及び機械的に研磨することを特徴とするケミカルメカニカルポリッシュ法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、Ａｇ（銀）を配線材料として用いた半導体装置の配線構造及び配線形成方法、銀薄膜形成方法、並びにかかる配線構造の形成に適したＣＶＤ装置及びケミカルメカニカルポリッシュ法に関する。
【０００２】
【従来の技術】半導体装置の高集積化に伴い、半導体装置の製造プロセスの寸法ルールが微細化し、これに伴い、半導体装置における配線幅も微細化してきている。現在、配線材料として、純アルミニウムあるいはアルミニウム合金（以下、これらを総称してＡｌ系合金とも呼ぶ）が主に用いられている。そして、例えば、絶縁層から成る下地上に所謂高温アルミニウムスパッタ法にてＡｌ系合金から成る金属配線層を形成した後、かかる金属配線層をフォトリソグラフィ技術及びエッチング技術によって所望のパターン形状にする。これによって、Ａｌ系合金から成る配線が形成される。その後、配線上に絶縁膜を形成し、かかる絶縁膜の平坦化処理を行う。
【０００３】金属配線層上にフォトリソグラフィ技術によってレジストパターンを形成するためには、露光時、金属配線層による光の乱反射を抑える必要がある。露光時に光の乱反射が抑えられない場合、光の乱反射の影響でハレーションが生じ、形成されたレジストパターンにはレジストの段切れ等の欠陥が生じる。従って、通常、例えばＴｉＯＮから成る反射防止膜を金属配線層上に形成した後、レジストパターニングを行っている。
【０００４】以下、高温アルミニウムスパッタ法及び研磨による平坦化処理法に基づいた従来の半導体素子の製造プロセス例を、図２０、図２１及び図２２を参照して説明する。
【０００５】［工程－１０］半導体基板から成る基体１００に素子分離領域１０２及びゲート領域１０４を形成する。その後、ＬＤＤイオン注入を行い、ゲートサイドウオール１０６を形成し、イオン注入を行ってソース・ドレイン領域１０８を形成する（図２０の（Ａ）参照）。
【０００６】［工程－２０］その後、全面に層間絶縁層１１２を形成し、次いで、層間絶縁層１１２に開口部１１４を形成する（図２０の（Ｂ）参照）。
【０００７】［工程－３０］次に、スパッタ法にて開口部１１４を含む層間絶縁層１１２の全面にＴｉ／ＴｉＮ／Ｔｉから成る密着層１１６を形成した後、高温アルミニウムスパッタ法にてＡｌ系合金（例えば、Ａｌ－１ｗｔ％Ｓｉ）から成る金属配線層１１８を全面に堆積させる。その後、全面にＴｉＯＮから成る反射防止膜１２０を形成する。そして、反射防止膜１２０、金属配線層１１８及び密着層１１６をフォトリソグラフィ技術及びドライエッチング技術によってパターニングすることにより、配線を形成する（図２０の（Ｃ）参照）。
【０００８】［工程－４０］次いで、研磨による平坦化処理を施す。即ち、配線を含む層間絶縁層１１２の全面にプラズマＣＶＤ法にてSiO_2から成る第１の絶縁膜１２２を形成し、その上にプラズマＣＶＤ法にてＳｉＮから成るストッパー層１２４を形成し、更にその上に厚いSiO_2から成る第２の絶縁膜１２６をＣＶＤ法にて形成する（図２１の（Ａ）参照）。
【０００９】［工程－５０］その後、上方から第２の絶縁膜１２６を研磨する。そしてストッパー層１２４が研

磨面として現れるまで研磨を行う（図２１の（Ｂ）参照）。こうして、配線の上に平坦化された第１の絶縁膜１２２を形成する。

【００１０】あるいは又、ＳｉＮから成るストッパー層１２４を用いる［工程－４０］及び［工程－５０］の代わりに、以下の工程にて平坦化処理された絶縁膜を形成することもできる。

【００１１】［工程－４０’］プラズマＣＶＤ法にてＳｉO_2から成る絶縁膜１３０を形成する。

【００１２】［工程－５０’］その後、絶縁膜１３０上にレジスト１３２を形成し、絶縁膜１３０の凸部が露出するようにレジスト１３２をパターニングする（図２２の（Ａ）参照）。

【００１３】［工程－６０’］次に、絶縁膜１３０の凸部をエッチングした後、レジスト１３２を除去する（図２２の（Ｂ）参照）。

【００１４】［工程－７０’］その後、エッチングされずに残った絶縁膜１３０の一部分１３０Ａを研磨して、絶縁膜１３０の平坦化を行う。

【００１５】

【発明が解決しようとする課題】配線が微細化すると、目的とする配線幅を制御性良く形成することは困難になる。下地である層間絶縁層１１２の凹凸の影響を受けて金属配線層１１８の表面には凹凸が生じる。また、Ａｌ系合金から成る金属配線層１１８を高温アルミニウムスパッタ法等にて形成したとき、金属配線層１１８の表面は荒れ易い（即ち、凹凸が形成され易い）。これらに起因して、金属配線層１１８の凹部内における反射防止膜１２０のカバレッジが低下する（例えば、図２０の（Ｃ）参照）。その結果、その部分での光の反射率が低下するために光の乱反射が生じ、結果としてハレーション等の影響で金属配線層１１８に対して目的のパターニング形状を形成できなくなる。

【００１６】また、レジストパターニング後の配線構造は、上からＴｉＯＮから成る反射防止膜１２０／金属配線層１１８である。レジストパターニング後、ドライエッチングによって金属配線層１１８のパターニングを行う。この場合、通常、エッチングガスとしてＢＣｌ$_3$系ガスを用いる。ところが、ＢＣｌ$_3$系ガスでのエッチングはケミカル反応のみであり、ＢＣｌ$_3$系ガスによってＴｉＯＮから成る反射防止膜１２０をエッチングすることは不可能である。それ故、物理的なスパッタ作用で反射防止膜１２０をエッチングする必要がある。

【００１７】そのため、Ａｌ系合金から成る金属配線層１１８をエッチングする際に、スパッタ作用を有するエッチング条件からケミカルエッチング条件へと変更する必要がある。ところが、反射防止膜１２０／金属配線層１１８の膜厚が不均一な場合、このようなエッチング条件の変更により、これらのエッチングが不均一となる。

【００１８】更に、ＳｉＮから成るストッパー層１２４を用いる［工程－４０］及び［工程－５０］で説明した方法は以下の問題点を有する。即ち、ＳｉO_2から成る第２の絶縁膜１２６を研磨する際にストッパー層１２４を用いているが、ＳｉO_2とＳｉＮの研磨に対する選択比は３～６程度しか得られない。そのため、ＳｉＮから成るストッパー層１２４が研磨の終点判定を行うべくストッパーとして機能せず、第１の絶縁膜１２２を研磨し過ぎる場合がある。即ち、制御性良く第２の絶縁膜１２６を研磨することができない。その結果、第１の絶縁膜１２２の完全な平坦化が達成できないという問題を有する。

【００１９】しかも、ＣＶＤ法等によってＳｉO_2若しくはＳＯＧから成る第１の絶縁膜１２２で配線間を埋め込む際、配線の間隔が細いと、第１の絶縁膜１２２の埋め込みが不十分となり、配線間の第１の絶縁膜１２２に「す（ボイド）」１２２Ａが発生するという問題も有している（図２３参照）。

【００２０】一方、ＳｉＮから成るストッパー層１２４を用いない［工程－４０’］～［工程－７０’］で説明した方法においても、絶縁膜１３０の研磨時、絶縁膜１３０の研磨の終点判定を行っていない。このため、絶縁膜１３０を研磨し過ぎるという問題を有する。

【００２１】このように微細な半導体装置の製造においては、配線を形成した後その上に平坦な絶縁膜を形成する従来の方法は上述のような種々の問題点を有しており、これらの問題点を効果的に解決するための方法は未だ無い。

【００２２】上記のプロセスにおいては、配線材料としてＡｌ系合金を用いている。Ａｌ系合金から成る金属配線層１１８においては、エレクトロマイグレーションが大きな問題である。また、金属配線層１１８のドライエッチング時、金属配線層のコロージョンによって金属配線層にボイドが発生し、配線の信頼性低下を招く。特に、微細配線化が進むに従い、配線に電流を流したとき金属配線層１１８中のアルミニウム粒子が移動する結果、金属配線層に発生した微小な欠けボイドに電流集中が生じる。そのため、エレクトロマイグレーションと欠けボイドの複合作用によって、配線の一層の信頼性低下を招いている。

【００２３】かかる問題を解決する一手段として銅（Ｃｕ）を配線材料として用いることが提案されている。しかしながら、Ｃｕの適切なエッチング方法が無くＣｕの加工性が良くないこと、非常に酸化され易く酸素を数％含む炉内での熱処理を行うことができないこと等、種々の問題を有している。加工性の問題は、絶縁層に溝部を形成し、かかる溝部を含む絶縁層上にＣｕを堆積させた後、絶縁層上のＣｕをケミカルメカニカルポリッシュ法にて化学的・機械的に研磨することによって回避することができる。しかしながら、溝部に埋め込まれたＣｕの表面の酸化を防止する有効な手段は知られていない。

【００２４】従って、本発明の第１の目的は、配線を形成するためのフォトリソグラフィ技術及びドライエッチング技術による金属配線層のパターニング工程を行う必要がなく、しかも、従来のように配線上に形成された絶縁膜の研磨を行わずに、配線を含む絶縁層の完全なる平坦化を可能とし、更にはＡｌ系合金やＣｕを配線材料として用いた場合の問題点を解決できる、新規の半導体装置の配線構造及び配線形成方法を提供することにある。

【００２５】本発明の第２の目的は、新規の銀薄膜形成方法を提供することにある。更に、本発明の第３の目的は、かかる配線構造及び配線形成方法への適用に適したＣＶＤ装置並びにケミカルメカニカルポリッシュ法を提供することにある。

【００２６】

【課題を解決するための手段】上記の第１の目的を達成するための本発明の第１の態様に係る半導体装置の配線構造は、（イ）基体上の絶縁層に形成された溝部又は開口部と、（ロ）溝部又は開口部内に形成された、下から密着層及びＡｇ層から成る多層の金属配線層、から構成されていることを特徴とする。

【００２７】本発明の第１の態様に係る半導体装置の配線構造においては、密着層を、Ｔｉ層、ＴｉＮ層、下からＴｉ層／ＴｉＮ層の２層構造、若しくは下からＡｇ層／Ｔｉ層の２層構造から構成することができる。また、溝部又は開口部の側壁に、金属配線層の酸化を防止するために、ＳｉＮから成るサイドウオールを形成してもよい。

【００２８】上記の第１の目的を達成するための本発明の第１の態様に係る半導体装置の配線形成方法は、

（イ）基体上に絶縁層を形成した後、絶縁層に溝部又は開口部を形成する工程と、（ロ）溝部又は開口部内を含む絶縁層上に、下から密着層及びＡｇ層から成る多層の金属配線層を形成する工程と、（ハ）絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残す工程、から成ることを特徴とする。

【００２９】本発明の第１の態様に係る半導体装置の配線形成方法においては、Ａｇ層の形成は、Ag_2CO_3、$AgNO_2$、ＡｇＢｒ若しくはＡｇＩを原料として用いた化学気相析出法にて行うことができる。（ハ）の工程における絶縁層上の金属配線層の除去は、金属配線層のケミカルメカニカルポリッシュ工程、あるいは、金属配線層のエッチバック工程から構成することができる。ケミカルメカニカルポリッシュ法においては、I_2とＫＩの混合水溶液を用いてＡｇ層のケミカルメカニカルポリッシュすることができる。

【００３０】また、密着層は、Ｔｉ層、ＴｉＮ層、下からＴｉ層／ＴｉＮ層の２層構造、若しくは下からＡｇ層／Ｔｉ層の２層構造から構成することができる。（イ）の工程の後に、溝部又は開口部の側壁にＳｉＮから成るサイドウオールを形成する工程を更に含ませることができる。

【００３１】上記の第１の目的を達成するための本発明の第２の態様に係る半導体装置の配線構造は、（イ）基体上の絶縁層に形成された溝部又は開口部と、（ロ）溝部又は開口部内に形成された、下から密着層、Ｃｕ層及びＡｇ層から成る多層の金属配線層、から構成されていることを特徴とする。

【００３２】本発明の第２の態様に係る半導体装置の配線構造においては、密着層は、Ｔｉ層、ＴｉＮ層、下からＴｉ層／ＴｉＮ層の２層構造、若しくは下からＡｇ層／Ｔｉ層の２層構造から構成することができる。また、溝部又は開口部の側壁に、ＳｉＮあるいは又Ａｇから成るサイドウオールを形成してもよい。

【００３３】上記の第１の目的を達成するための本発明の第２の態様に係る半導体装置の配線形成方法は、

（イ）基体上に絶縁層を形成した後、絶縁層に溝部又は開口部を形成する工程と、（ロ）溝部又は開口部内を含む絶縁層上に、下から密着層、Ｃｕ層及びＡｇ層から成る多層の金属配線層を形成する工程と、（ハ）絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残す工程、から成ることを特徴とする。

【００３４】本発明の第２の態様に係る半導体装置の配線形成方法においては、（ハ）の工程における絶縁層上の金属配線層の除去は、金属配線層のケミカルメカニカルポリッシュ工程から構成することができる。この場合、ケミカルメカニカルポリッシュによるＡｇ層の除去は、I_2とＫＩの混合水溶液を用いて行う。あるいは又、（ハ）の工程における絶縁層上の金属配線層の除去は、金属配線層のエッチバック工程から構成することができる。

【００３５】上記の第１の目的を達成するための本発明の第３の態様に係る半導体装置の配線形成方法は、

（イ）基体上に絶縁層を形成した後、絶縁層に溝部又は開口部を形成する工程と、（ロ）溝部又は開口部内を含む絶縁層上に、下から密着層及びＣｕ層から成る多層の第１の金属配線層を形成する工程と、（ハ）絶縁層上の第１の金属配線層を除去し、溝部又は開口部内に第１の金属配線層を残す工程と、（ニ）絶縁層上及び第１の金属配線層上に、Ａｇ層から成る第２の金属配線層を形成する工程と、（ホ）絶縁層上の第２の金属配線層を除去し、溝部又は開口部内に第２の金属配線層を残す工程、から成ることを特徴とする。

【００３６】本発明の第３の態様に係る半導体装置の配線形成方法においては、（ハ）の工程における絶縁層上の第１の金属配線層の除去、又は、（ホ）の工程における絶縁層上の第２の金属配線層の除去は、ケミカルメカニカルポリッシュ工程から構成することができる。この場合、ケミカルメカニカルポリッシュによるＡｇ層の除去は、I_2とＫＩの混合水溶液を用いて行う。あるいは又、（ハ）の工程における絶縁層上の第１の金属配線層

の除去、又は、（ホ）の工程における絶縁層上の第２の金属配線層の除去は、エッチバック工程から構成することができる。

【００３７】本発明の第２又は第３の態様に係る半導体装置の配線形成方法においては、密着層は、Ｔｉ層、ＴｉＮ層、下からＴｉ層／ＴｉＮ層の２層構造、若しくは下からＡｇ層／Ｔｉ層の２層構造から構成することができる。また、（イ）の工程の後に、溝部又は開口部の側壁にＳｉＮあるいはＡｇから成るサイドウオールを形成する工程を更に含むことができる。

【００３８】上記の第２の目的を達成するための銀薄膜の形成方法は、Ag_2CO_3を原料として用いた化学気相析出法によることを特徴とする。あるいは又、$AgNO_2$を原料として用いた化学気相析出法によることを特徴とする。更には、ＡｇＢｒを原料として用いた化学気相析出法によることを特徴とする。更には、ＡｇＩを原料として用いた化学気相析出法によることを特徴とする。これらの原料をガス化して不活性ガス等のキャリアガスを用いてＣＶＤガスとして用いる。

【００３９】上記の第３の目的を達成するための本発明のＣＶＤ装置は、原料源と、ＣＶＤチャンバと、原料源とＣＶＤチャンバとを結ぶ配管とを備えている。そして、配管を原料の沸点以上に加熱する第１のヒーターと、原料をＣＶＤチャンバに導入するためのＣＶＤチャンバ導入部を原料の沸点以上に加熱する第２のヒーターとを備えていることを特徴とする。第２のヒーターをランプ加熱装置とすることができる。

【００４０】上記の第３の目的を達成するためのケミカルメカニカルポリッシュ法は、I_2及びＫＩの混合水溶液を用いて銀薄膜を化学的及び機械的に研磨することを特徴とする。

【００４１】

【作用】本発明においては、溝部又は開口部内に金属配線層が形成されている。このような形態の金属配線層は、絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残すことによって形成されるので、従来技術のようにフォトリソグラフィ技術及びドライエッチング技術によって絶縁層上に形成された金属配線層のパターニングを行う必要がない。また、絶縁層上の金属配線層の除去による平坦化処理を行うので、従来の技術のような配線上に形成された絶縁膜の平坦化処理を行う必要がない。

【００４２】Ａｇは高温熱処理で酸化され難い。Ａｇも酸化するが１００°Ｃ以上の温度でＡｇＯ→Ａｇ＋Ｏに分解する。このため数百°Ｃの温度でＡｇＯは安定化せず、Ａｇの酸化物を保たない。また、Ａｇから金属配線層を構成するので、Ａｌ系合金のようなエレクトロマイグレーションの問題は発生しない。従って、本発明の第１の態様に係る配線構造あるいは配線形成方法においては、安定した配線を形成することができる。

【００４３】本発明の第２の態様に係る配線構造あるいは第２又は第３の態様に係る配線形成方法においては、Ａｇ層及びＣｕ層から金属配線層を構成するので、Ａｌ系合金のようなエレクトロマイグレーションの問題は発生しない。しかも、Ｃｕ層の表面はＡｇ層で被覆されているので、Ｃｕ層の酸化を防止することができる。

【００４４】以下、図面を参照して、実施例に基づき本発明を説明する。尚、実施例１～実施例６においては、本発明の第１の態様に係る半導体装置の配線構造及び第１の態様に係る配線形成方法を説明する。また、実施例７～実施例１２においては、本発明の第２の態様に係る半導体装置の配線構造及び第２の態様に係る配線形成方法を説明する。更に、実施例１３～実施例１５においては、本発明の第２の態様に係る半導体装置の配線構造及び第３の態様に係る配線形成方法を説明する。

【００４５】（実施例１）実施例１～実施例６は、本発明の第１の態様に係る半導体装置の配線構造及び第１の態様に係る配線形成方法に関する。図１に半導体装置の模式的な一部断面図を示すように、実施例１の配線構造は、基体１０上の絶縁層１２に形成された溝部１４、溝部１４内に形成された多層の金属配線層２２から成る。金属配線層２２は、下から密着層１６及びＡｇ層２０から構成されている。密着層１６は、下からＴｉ層１８Ａ／ＴｉＮ層１８Ｂの２層構造である。

【００４６】実施例１の配線形成方法は、（イ）基体１０上に絶縁層１２を形成した後、絶縁層１２に溝部１４を形成する工程と、（ロ）溝部１４内を含む絶縁層１２上に、下から密着層１６及びＡｇ層２０から成る多層の金属配線層２２を形成する工程と、（ハ）絶縁層１２上の金属配線層２２を除去し、溝部１４内に金属配線層２２を残す工程から成る。Ａｇ層２０の形成は、Ag_2CO_3を原料として用いた化学気相析出法による。また、（ハ）の工程における絶縁層１２上の金属配線層２２の除去は、I_2とＫＩの混合水溶液を用いた金属配線層２２のケミカルメカニカルポリッシュ工程から成る。SiO_2から成る絶縁層１２をストッパーとして機能させることにより、ケミカルメカニカルポリッシュに対する金属配線層２２と絶縁層１２の選択比を無限大まで設定することが可能となる。

【００４７】以下、半導体装置等の模式的な一部断面図である図２を参照して、実施例１の配線形成方法を具体的に説明する。

【００４８】［工程－１００］例えば半導体基板から成る基体１０上にSiO_2から成る絶縁層１２を形成する。絶縁層１２の形成条件を、例えば以下のとおりとすることができる。

使用ガス　　：　SiH_4／O_2／N_2＝２５０／２５０／１００sccm

基板加熱温度：　４２０°Ｃ

圧力　　：　１３．３Ｐａ

膜厚　　：　０．８μｍ

【００４９】［工程－１１０］その後、フォトリソグラフィ技術及びドライエッチング技術によって、絶縁層１２に溝部１４を形成する（図２の（Ａ）参照）。尚、溝部１４は図２の紙面に垂直な方向に延びている。ドライエッチングの条件を、例えば以下のとおりとすることができる。

使用ガス　：　C_4F_8＝５０sccm
ＲＦパワー　：　１２００Ｗ
圧力　　：　２Ｐａ

【００５０】［工程－１２０］次に、下からＴｉ層１８Ａ／ＴｉＮ層１８Ｂから成る密着層１６を溝部１４を含む絶縁層１２上にスパッタ法にて形成する（図２の（Ｂ）参照）。密着層１６を、例えば以下の条件で形成することができる。

Ｔｉ層１８Ａの形成
使用ガス　：　Ａｒ＝１００sccm
パワー　　：　４ｋＷ
圧力　　：　０．４７Ｐａ
成膜温度　：　１５０°Ｃ
膜厚　　：　５０ｎｍ
ＴｉＮ層１８Ｂの形成
使用ガス　：　Ａｒ／N_2＝４０／７０sccm
パワー　　：　５ｋＷ
圧力　　：　０．４７Ｐａ
膜厚　　：　７０ｎｍ

【００５１】［工程－１３０］その後、銀（Ａｇ）層２０をＣＶＤ法にて全面に形成する（図２の（Ｃ）参照）。Ａｇ層２０の形成は、Ag_2CO_3を原料として用いた化学気相析出法による。ＣＶＤの条件を、例えば以下のとおりとすることができる。

原料　　：　Ag_2CO_3
原料源温度　：　１７０°Ｃ
使用ガス　：　Ag_2CO_3／Ａｒ／H_2＝１０／２５／１０００sccm
圧力　　：　2.6×10^3Ｐａ
基板加熱温度：　４５０°Ｃ

これによって、溝部１４内を含む絶縁層１２上にＡｇ層２０が堆積する。Ａｇ層２０は下記の反応によって形成される。

$Ag_2CO_3+H_2\rightarrow2Ag+CO_2\uparrow+H_2O\uparrow$

【００５２】Ａｇ層２０の形成のために、図３に示す本発明のＣＶＤ装置を使用した。このＣＶＤ装置は、ＣＶＤチャンバ２００と、原料源２０２と、原料源とＣＶＤチャンバとを結ぶ配管２０４とを備えている。そして、配管２０４を原料の沸点以上に加熱する第１のヒーター２０６と、原料をＣＶＤチャンバに導入するためのＣＶＤチャンバ導入部２０８を原料の沸点以上に加熱する第２のヒーター２１０とを備えている。第２のヒーター２１０はランプ加熱装置であり、ミラー２１２が設けられている。また、第２のヒーター２１０と対抗するＣＶＤチャンバ導入部２０８近傍の配管２０４の部分には石英製の窓２１４が設けられている。尚、図３中、２１６は基体１０を加熱するためのランプ加熱装置、２１８は不活性ガス導入部、２２０は原料源２０２を加熱するためのヒーターである。第１及び第２のヒーター２０６，２１０によって、配管２０４及びＣＶＤチャンバ導入部２０８内を流れるAg_2CO_3ガスは沸点である２１８°Ｃ以上に保持される。

【００５３】［工程－１４０］次に、ケミカルメカニカルポリッシュ法によって絶縁層１２上のＡｇ層２０及び密着層１６を化学的及び機械的に研磨して除去し、溝部１４内にＡｇ層２０及び密着層１６を残し、金属配線層２２から成る配線を形成する（図１参照）。ケミカルメカニカルポリッシュには、図４に示す研磨装置を用いる。ケミカルメカニカルポリッシュの条件を、例えば以下のとおりとすることができる。

研磨プレート回転数　：　３７ｒｐｍ
基板保持台回転数　：　１７ｒｐｍ
研磨圧力　　：　5.5×10^8Ｐａ
パッド温度　　：　４０°Ｃ

I_2＋ＫＩの混合水溶液を用いて、ケミカルメカニカルポリッシュを行う。

【００５４】従来SiO_2を研磨する場合はスラリー（SiO_2系の研磨剤＋ＫＯＨ＋水）を用いるが、スラリーでSiO_2を研磨する際、スラリーが研磨すべき面内に均一に分布しないため、研磨し過ぎ等により基板内の研磨面の平坦化にばらつきが生じるという問題がある。Ａｇ層２０及び密着層１６を研磨する場合、スラリーを必要とせず、I_2＋ＫＩの混合水溶液で研磨することで、Ａｇ層２０及び密着層１６のみを除去することが可能であり、基板内の研磨面の平坦化にばらつきも少ないという利点を有する。

【００５５】これによって、平坦な絶縁層１２に埋め込まれた金属配線層２２から成る配線が形成される。実施例１においては、従来の配線形成方法のように金属配線層のレジストパターニング処理及びドライエッチング処理が不要となり、レジストパターニング時の光の散乱の問題、エッチングが不均一となる問題を回避することができる。また、配線上の絶縁膜の形成及びかかる絶縁膜の平坦化処理も不要である。

【００５６】（実施例２）実施例１では、絶縁層１２上のＡｇ層２０及び密着層１６から成る金属配線層２２の除去をケミカルメカニカルポリッシュ法にて行った。実施例２においては、その代わりに、ドライエッチングによるエッチバック法にて金属配線層２２を除去する。尚、その他の工程は実施例１と同様であり、詳細な説明は省略する。

【００５７】［金属配線層２２のエッチング工程］溝部１４を含む絶縁層１２上に形成されたＡｇ層２０及び密

着層１６を、例えば以下の条件のドライエッチング法にてエッチバックし、溝部１４内に密着層１６及びＡｇ層２０から成る金属配線層２２を残す。

使用ガス　　：　NO_2／O_2＝２０／２０sccm
マイクロ波パワー：　８５０Ｗ
ＲＦパワー　　：　１０Ｗ
圧力　　：　１．３Ｐａ
基板加熱温度　　：　１００°Ｃ

【００５８】（実施例３）実施例３においては、実施例１の［工程－１１０］と［工程－１２０］との間に、溝部１４の側壁にＳｉＮから成るサイドウオール２６を形成する工程を更に含む。尚、その他の工程は実施例１と同様であり、詳細な説明は省略する。以下、実施例３のサイドウオール２６の形成工程を、図５を参照して説明する。サイドウオール２６を形成することによって、絶縁層１２による密着層１６の酸化を防止することができる。

【００５９】［サイドウオール２６の形成工程］溝部１４内を含む絶縁層１２上の全面にプラズマＣＶＤ法にてＳｉＮ層２６Ａを堆積させる（図５の（Ａ）参照）。ＳｉＮ層２６Ａの形成条件を、以下に例示する。

使用ガス：　SiH_4／NH_3／N_2＝１８０／５００／７２０sccm
温度　　：　２００°Ｃ
圧力　　：　４０Ｐａ
膜厚　　：　１００ｎｍ

【００６０】その後、ＳｉＮ層２６Ａを全面エッチバックする（図５の（Ｂ）参照）。エッチバックの条件を、例えば以下のとおりとすることができる。

使用ガス　　：　CHF_3＝５０sccm
ＲＦパワー　：　３００Ｗ
圧力　　：　２Ｐａ

これによって、溝部１４の側壁にサイドウオール２６が形成される。以降、実施例１の［工程－１２０］～［工程－１４０］を経て、図５の（Ｃ）に示す配線構造を形成することができる。

【００６１】（実施例４）図６に模式的な一部断面図を示す実施例４の配線構造は、実施例１と若干異なり、半導体基板から成る基体１０上の第１の絶縁層１２Ａに形成された開口部１４Ａと、第１の絶縁層１２Ａ上に形成された第２の絶縁層１２Ｂに形成された溝部１４Ｂと、開口部１４Ａ及び溝部１４Ｂに埋め込まれた密着層１６及びＡｇ層２０から成る金属配線層２２から構成されている。この場合、開口部１４Ａの側壁及び溝部１４Ｂの側部にＳｉＮから成るサイドウオール２６を形成してもよい。また、開口部１４Ａを金属配線層２２で埋め込むことによって、下層導体層（例えば、ソース・ドレイン領域３６）と溝部１４Ｂ内の配線２４とが電気的に接続される。

【００６２】実施例４の配線形成方法は、実施例１と若干異なり、予め半導体基板から成る基体１０上の第１の絶縁層１２Ａに開口部１４Ａを、また、第１の絶縁層１２Ａ上に形成された第２の絶縁層１２Ｂに溝部１４Ｂを形成した後、密着層１６及びＡｇ層２０から成る金属配線層２２で開口部１４Ａ及び溝部１４Ｂを埋め込み配線構造を形成する。第２の絶縁層１２Ｂ上の金属配線層２２はケミカルメカニカルポリッシュ法にて除去される。以下、半導体装置等の模式的な一部断面図である図７及び図８を参照して、実施例４の配線形成方法を説明する。

【００６３】［工程－４００］Ｓｉ（１００）から成る半導体基板から成る基体１０上に、通常の方法で素子分離領域３０及びゲート領域３２を形成する。次いで、ＬＤＤイオン注入を行った後、全面にゲートサイドウオール３４を形成するためにSiO_2膜を堆積させる。SiO_2膜の堆積条件を、例えば以下のとおりとすることができる。

使用ガス　：　SiH_4／O_2／N_2＝２５０／２５０／１００sccm
温度　　：　４２０°Ｃ
圧力　　：　１３．３Ｐａ
膜厚　　：　０．２５μｍ

更に、SiO_2膜の全面エッチバックを行い、ゲート領域３２の側壁にゲートサイドウオール３４を形成する。全面エッチバックを、例えば以下の条件で行うことができる。

使用ガス　：　C_4F_8＝５０sccm
ＲＦパワー：　１２００Ｗ
圧力　　：　２Ｐａ

その後、ソース・ドレイン領域３６の形成のために、不純物イオン注入を、例えば以下の条件にて行う。

Ｎ型チャネルの形成
Ａｓ　２０ＫｅＶ，５×10^{15}／cm^2
Ｐ型チャネルの形成
BF_2　２０ＫｅＶ，３×10^{15}／cm^2

こうして、図７の（Ａ）に模式的な一部断面図で示す構造を得ることができる。

【００６４】［工程－４１０］その後、SiO_2及びＢＰＳＧの２層から成る第１の絶縁層１２Ａを、例えば以下の条件のＣＶＤ法にて全面に形成する。

SiO_2層の形成
使用ガス　：　ＴＥＯＳ　５０sccm
圧力　　：　４０Ｐａ
温度　　：　７２０°Ｃ
膜厚　　：　４００ｎｍ

ＢＰＳＧ層の形成
使用ガス　：　SiH_4／PH_3／B_2H_6／O_2／N_2＝８０／７／７／１０００／３２０００sccm
温度　　：　４００°Ｃ
圧力　　：　１．０×10^5Ｐａ

膜厚　　：　５００ｎｍ
更に９００°Ｃ、２０分のリフロー処理を行い、第１の絶縁層１２Ａの平坦化を行う。
【００６５】［工程－４２０］次に、SiO_2から成る第２の絶縁層１２Ｂを全面に形成する。第２の絶縁層１２Ｂを、例えば以下の条件で形成することができる。
使用ガス　：　SiH_4／O_2／N_2＝２５０／２５０／１００sccm
温度　　：　４２０°Ｃ
圧力　　：　１３．３Ｐａ
膜厚　　：　０．８μｍ
【００６６】［工程－４３０］その後、実施例１の［工程－１１０］と同様に、フォトリソグラフィ技術及びドライエッチング技術によって、第２の絶縁層１２Ｂに溝部１４Ｂを形成する（図７の（Ｂ）参照）。
【００６７】［工程－４４０］次いで、レジストパターニング後ドライエッチングを行うことによって、第１の絶縁層１２Ａに開口部１４Ａを形成する（図７の（Ｃ）参照）。ここで、溝部１４Ｂの幅を開口部１４Ａの径よりも大きくする。ドライエッチングの条件を、例えば以下のとおりとすることができる。
使用ガス　：　C_4F_8　５０sccm
ＲＦパワー：　１２００Ｗ
圧力　　：　２Ｐａ
更に、開口部内にイオン注入を行うことにより、接合領域を形成した後、１１００°Ｃ、１０秒の活性化アニールを行う。イオン注入の条件として、以下の例を挙げることができる。
Ｎ型チャネルの形成
Ａｓ　２０ＫｅＶ，5×10^{15}／cm^2
Ｐ型チャネルの形成
BF_2　２０ＫｅＶ，3×10^{15}／cm^2
【００６８】［工程－４５０］その後、実施例３の［サイドウオール２６の形成工程］と同様に、全面にプラズマＣＶＤ法にてＳｉＮ層を形成し、次いで、ＳｉＮ層を全面エッチバックして、開口部１４Ａの側壁及び溝部１４Ｂの側壁にＳｉＮから成るサイドウオール２６を形成することが望ましい（図８の（Ａ）参照）。
【００６９】［工程－４６０］次に、下からＴｉ層／ＴｉＮ層から成る密着層１６を開口部１４Ａ及び溝部１４Ｂを含む第２の絶縁層１２Ｂ上にスパッタ法にて形成する。この工程は、実施例１の［工程－１２０］と同様とすることができる。
【００７０】［工程－４７０］その後、実施例１の［工程－１３０］と同様に、Ag_2CO_3を原料として用いた化学気相析出法によって、Ａｇ層２０を全面に形成する（図８の（Ｂ）参照）。
【００７１】［工程－４８０］次に、実施例１の［工程－１４０］と同様に、ケミカルメカニカルポリッシュ法によって第２の絶縁層１２Ｂ上のＡｇ層２０及び密着層１６を化学的及び機械的に研磨して除去し、溝部１４Ｂ内及び開口部１４Ａ内にＡｇ層２０及び密着層１６を残し、金属配線層２２から成る接続孔及び配線を形成する（図６参照）。即ち、開口部１４Ａ内に金属配線層２２が埋め込まれた接続孔（例えば、所謂コンタクトホール）が形成される。また、溝部１４Ｂに金属配線層２２が埋め込まれた配線２４が形成される。
【００７２】尚、Ａｇ層２０及び密着層１６から成る金属配線層２２をケミカルメカニカルポリッシュ法にて除去する代わりに、実施例２と同様にドライエッチング法にてエッチバックすることで除去することもできる。
【００７３】（実施例５）実施例５は、実施例４の変形である。実施例５の配線構造は実施例４と同様であるが、配線形成方法が実施例４と相違する。即ち、第１の絶縁層１２Ａに設けられた開口部１４ＡをＡｇから成る金属配線材料で埋め込み接続孔２４Ａを完成させ、次いで、その上に第２の絶縁層１２Ｂを堆積させ、かかる第２の絶縁層１２Ｂに溝部１４Ｂを形成する点が実施例４と相違する。実施例５においては、実施例４の［工程－４００］、［工程－４１０］及び［工程－４４０］は同様の工程であり、その他の工程が異なる。以下、図９及び図１０を参照して、実施例５の方法を説明する。
【００７４】
［工程－５００］～［工程－５２０］Ｓｉ（１００）の半導体基板から成る基体１０上に、通常の方法で素子分離領域３０及びゲート領域３２を形成する。次いで、ＬＤＤイオン注入を行った後、ゲートサイドウオール３４を形成し、ソース・ドレイン領域３６の形成のために、不純物イオン注入を行う。その後、SiO_2及びＢＰＳＧの２層から成る第１の絶縁層１２Ａを、例えばＣＶＤ法にて全面に形成し、リフロー処理を行い、第１の絶縁層１２Ａの平坦化を行う。次いで、第１の絶縁層１２Ａに、レジストパターニング後ドライエッチングにて開口部１４Ａを形成し、開口部内にイオン注入を行うことにより、接合領域を形成させた後、活性化アニールを行う。これらの工程は、実施例４の［工程－４００］、［工程－４１０］及び［工程－４４０］と同様とすることができる。次いで、ＳｉＮから成るサイドウオール（図示せず）を開口部１４Ａの側壁に形成してもよい。
【００７５】［工程－５３０］
［工程－５２０］の後、実施例１の［工程－１２０］と同様の方法で、下からＴｉ／ＴｉＮから成る第１の密着層１６Ａを全面に形成する。次いで、実施例１の［工程－１３０］と同様の方法で、第１のＡｇ層２０ＡをＣＶＤ法にて全面に成膜し、第１の密着層１６Ａと第１のＡｇ層２０Ａから成る第１の金属配線層を形成する（図９の（Ａ）参照）。
【００７６】［工程－５４０］その後、ケミカルメカニカルポリッシュ法にて第１の絶縁層１２Ａ上の第１の金属配線層を除去し、開口部１４Ａ内のみに第１の金属配

線層２０Ａ，１６Ａを残す（図９の（Ｂ）参照）。ケミカルメカニカルポリッシュの条件は、実施例１の［工程－１４０］と同様とすることができる。これによって、開口部１４Ａに第１の金属配線層が埋め込まれた所謂コンタクトホール２４Ａが形成される。ケミカルメカニカルポリッシュ法の代わりに、実施例２と同様に、ドライエッチング法によるエッチバックにて開口部１４Ａ内のみに第１の金属配線層２０Ａ，１６Ａを残してもよい。

【００７７】［工程－５５０］次いで、全面にSiO_2から成る第２の絶縁層１２Ｂを形成する。第２の絶縁層１２Ｂを、例えば実施例４の［工程－４２０］と同様の条件で形成することができる。その後、実施例４の［工程－４３０］と同様に、フォトリソグラフィ技術及びドライエッチング技術によって、第２の絶縁層１２Ｂに溝部１４Ｂを形成する（図１０の（Ａ）参照）。その後、必要に応じて、実施例４の［工程－４５０］と同様に、全面にプラズマＣＶＤ法にてＳｉＮ層を形成し、次いで、ＳｉＮ層を全面エッチバックし、これによって、溝部１４Ｂの側壁にＳｉＮから成るサイドウオール（図示せず）を形成してもよい。

【００７８】［工程－５６０］次に、実施例１の［工程－１２０］と同様の方法で、厚さ３０ｎｍのＴｉから成る第２の密着層１６Ｂを溝部１４Ｂを含む第２の絶縁層１２Ｂ上にスパッタ法にて形成した後、実施例１の［工程－１３０］と同様の方法で、第２のＡｇ層２０ＢをＣＶＤ法にて全面に成膜し、第２の密着層１６Ｂと第２のＡｇ層２０Ｂから成る第２の金属配線層を形成する。

【００７９】［工程－５７０］次いで、ケミカルメカニカルポリッシュ法によって第２の絶縁層１２Ｂ上の第２の金属配線層２０Ｂ，１６Ｂを除去し、溝部１４Ｂ内に第２のＡｇ層２０Ｂ及び第２の密着層１６Ｂを残し、配線２４を形成する（図１０の（Ｂ）参照）。ケミカルメカニカルポリッシュの条件は、実施例１の［工程－１４０］と同様とすることができる。

【００８０】尚、ケミカルメカニカルポリッシュ法によって第２の絶縁層１２Ｂ上の第２の金属配線層２０Ｂ，１６Ｂを除去する代わりに、実施例２と同様に、第２の金属配線層２０Ｂ，１６Ｂをドライエッチング法にてエッチバックし、これによって、溝部１４Ｂ内にのみ第２の金属配線層２０Ｂ，１６Ｂを残し、溝部１４Ｂ内に配線２４を形成することもできる。

【００８１】（実施例６）実施例６は実施例５の変形である。実施例６が実施例５と相違する点は、予め開口部１４Ａ内にＣＶＤ法にてタングステンプラグを形成する点にある。以下、図１１を参照して実施例６の配線形成方法を説明する。

【００８２】

［工程－６００］～［工程－６２０］これらの工程は、実施例５の［工程－５００］～［工程－５２０］と同様とすることができる。

【００８３】［工程－６３０］

［工程－６２０］の後、Ｔｉ／ＴｉＮから成るバリア層４０を全面にスパッタ法にて形成し、その後、全面にタングステン層４２をＣＶＤ法にて成膜する（図１１の（Ａ）参照）。Ｔｉ及びＴｉＮの成膜条件を、例えば実施例１の［工程－１２０］と同様とすることができる。また、ＣＶＤ法によるタングステンの成膜条件を、以下に例示する。

使用ガス　：　WF_6/H_2＝９５／５５０sccm
成膜温度　：　４５０°Ｃ
圧力　　：　１．１×10^4Ｐａ
膜厚　　：　０．４μｍ

【００８４】［工程－６４０］その後、ドライエッチング法にてエッチバックを行い、第１の絶縁層１２Ａ上のタングステン層４２及びバリア層４０を除去して、開口部１４Ａ内のみにタングステン層４２から成るメタルプラグ及びバリア層４０を残す（図１１の（Ｂ）参照）。ドライエッチングの条件は、例えば以下のとおりとすることができる。

使用ガス　　：　SF_6＝５０sccm
マイクロ波パワー：　８５０Ｗ
ＲＦパワー　　：　１５０Ｗ
圧力　　：　１．３３Ｐａ

これによって、開口部１４Ａにタングステンが埋め込まれた所謂タングステンプラグから成るコンタクトホール２４Ａが形成される。尚、ドライエッチング法によるエッチバックの代わりに、ケミカルメカニカルポリッシュ法によって開口部１４Ａ内のみにタングステン層４２及びバリア層４０を残してもよい。

【００８５】［工程－６５０］次いで、全面にSiO_2から成る第２の絶縁層１２Ｂを形成する。第２の絶縁層１２Ｂを、例えば実施例５の［工程－５５０］と同様の条件で形成することができる。その後、実施例５の［工程－５５０］と同様に、フォトリソグラフィ技術及びドライエッチング技術によって、第２の絶縁層１２Ｂに溝部１４Ｂを形成する。尚、溝部１４Ｂの幅を開口部１４Ａの径よりも大きくする。

【００８６】［工程－６６０］次に、実施例５の［工程－５６０］と同様の方法で、３０ｎｍ厚さのＴｉから成る密着層１６を溝部１４Ｂを含む第２の絶縁層１２Ｂ上にスパッタ法にて形成した後、実施例１の［工程－１３０］と同様の方法で、Ａｇ層２０をＣＶＤ法にて全面に成膜し、密着層１６とＡｇ層２０から成る金属配線層を形成する。

【００８７】［工程－６７０］その後、実施例１の［工程－１４０］と同様の方法で、第２の絶縁層１２Ｂ上の金属配線層をケミカルメカニカルポリッシュ法あるいはドライエッチングによるエッチバックにて除去する。これによって、溝部１４Ｂ内にのみ金属配線層を残し、溝部１４Ｂ内に密着層１６及びＡｇ層２０から成る金属配

線層から構成された配線２４を形成する（図１１の（Ｃ）参照）。

【００８８】（実施例７）実施例７～実施例１２は、本発明の第２の態様に係る半導体装置の配線構造及び第２の態様に係る配線形成方法に関する。図１２に半導体装置の模式的な一部断面図を示すように、実施例７の配線構造は、基体１０上の絶縁層１２に形成された溝部１４、溝部１４内に形成された多層の金属配線層５０から成る。金属配線層５０は、下から密着層５２、Ｃｕ層５４及びＡｇ層５６から構成されている。また、密着層５２は、下からＴｉ層５２Ａ／ＴｉＮ層５２Ｂの２層構造である。

【００８９】実施例７の配線形成方法は、（イ）基体１０上に絶縁層１２を形成した後、絶縁層１２に溝部１４を形成する工程と、（ロ）溝部１４を含む絶縁層１２上に、下から密着層５２、Ｃｕ層５４及びＡｇ層５６から成る多層の金属配線層５０を形成する工程と、（ハ）絶縁層１２上の金属配線層５０を除去し、溝部１４内に金属配線層を残す工程から成る。

【００９０】密着層５２、Ｃｕ層５４及びＡｇ層５６の形成はスパッタ法にて行う。また、（ハ）の工程における絶縁層１２上の金属配線層５０の除去は、金属配線層５０のケミカルメカニカルポリッシュ工程から成る。SiO_2から成る絶縁層１２をストッパーとして機能させることにより、ケミカルメカニカルポリッシュに対する金属配線層５０と絶縁層１２の選択比を無限大まで設定することが可能となる。

【００９１】以下、半導体装置等の模式的な一部断面図である図１３を参照して、実施例７の配線形成方法を具体的に説明する。

【００９２】［工程－７００］例えば半導体基板から成る基体１０上にSiO_2から成る絶縁層１２を形成する。絶縁層１２の形成条件を、例えば実施例１の［工程－１００］と同様とすることができる。その後、フォトリソグラフィ技術及びドライエッチング技術によって、絶縁層１２に溝部１４を形成する。尚、溝部１４は図１３の紙面に垂直な方向に延びている。ドライエッチングの条件を、実施例１の［工程－１１０］と同様とすることができる。

【００９３】［工程－７１０］次に、下からＴｉ層５２Ａ／ＴｉＮ層５２Ｂから成る密着層５２を溝部１４を含む絶縁層１２上にスパッタ法にて形成する（図１３の（Ａ）参照）。密着層５２を、例えば実施例１の［工程－１２０］と同様とすることができる。

【００９４】［工程－７２０］その後、銅（Ｃｕ）層５４をスパッタ法にて全面に形成する（図１３の（Ｂ）参照）。Ｃｕ層５４の形成を、例えば以下のスパッタ条件にて行うことができる。

使用ガス　：　Ａｒ＝１００sccm
パワー　　：　１０ｋＷ
圧力　　：　０．４７Ｐａ
成膜温度　：　２００°Ｃ
膜厚　　：　５００ｎｍ

【００９５】［工程－７３０］その後、銀（Ａｇ）層５６をスパッタ法にて全面に形成する（図１３の（Ｃ）参照）。Ａｇ層５６の形成を、例えば以下の条件のスパッタ法にて行うことができる。

使用ガス　：　Ａｒ＝１００sccm
パワー　　：　１０ｋＷ
圧力　　：　０．４７Ｐａ
成膜温度　：　２００°Ｃ
膜厚　　：　１００ｎｍ

こうしてＣｕ層５４の表面がＡｇ層５６で被覆される。

【００９６】［工程－７４０］次に、ケミカルメカニカルポリッシュ法によって絶縁層１２上のＡｇ層５６、Ｃｕ層５４及び密着層５２を化学的及び機械的に研磨して除去し、溝部１４内にＡｇ層５６、Ｃｕ層５４及び密着層５２を残し、金属配線層５０から成る配線を形成する（図１２参照）。ケミカルメカニカルポリッシュには、図４に示す研磨装置を用いる。ケミカルメカニカルポリッシュの条件を、例えば以下のとおりとすることができる。

研磨プレート回転数　：　３７ｒｐｍ
基板保持台回転数　：　１７ｒｐｍ
研磨圧力　：　５．５×10^8Ｐａ
パッド温度　：　４０°Ｃ

Ａｇ層５６のケミカルメカニカルポリッシュ法による除去にはI_2＋ＫＩの混合水溶液を用いる。また、Ｃｕ層５４及び密着層５２のケミカルメカニカルポリッシュ法による除去には$K_4Fe(CN)_6+H_2O$を用いる。

【００９７】従来SiO_2を研磨する場合はスラリー（SiO_2系の研磨剤＋ＫＯＨ＋水）を用いるが、スラリーでSiO_2を研磨する際、スラリーが研磨すべき面内に均一に分布しないため、研磨し過ぎ等により基板内の研磨面の平坦化にばらつきが生じるという問題がある。Ａｇ層５６、Ｃｕ層５４及び密着層５２を研磨する場合、スラリーを必要とせず、I_2＋ＫＩの混合水溶液、及び$K_4Fe(CN)_6$水溶液で研磨することで、Ａｇ層５６、Ｃｕ層５４及び密着層５２のみを除去することが可能であり、基板内の研磨面の平坦化にばらつきも少ないという利点を有する。

【００９８】これによって、平坦な絶縁層１２に埋め込まれた金属配線層５０から成る配線が形成される。実施例７においては、従来の配線形成方法のように金属配線層のレジストパターニング処理及びドライエッチング処理が不要となり、レジストパターニング時の光の散乱の問題、エッチングが不均一となる問題を回避することができる。また、配線上の絶縁膜の形成及びかかる絶縁膜の平坦化処理も不要である。

【００９９】（実施例８）実施例７では、絶縁層１２上

のＡｇ層５６、Ｃｕ層５４及び密着層５２から成る金属配線層５０の除去をケミカルメカニカルポリッシュ法にて行った。実施例２においては、その代わりに、ドライエッチングによるエッチバック法にて金属配線層５０を除去する。尚、その他の工程は実施例７と同様であり、詳細な説明は省略する。

【０１００】［金属配線層５０のエッチング工程］溝部１４を含む絶縁層１２上に形成されたＡｇ層５６、Ｃｕ層５４及び密着層５２を、例えば以下の条件のドライエッチング法にてエッチバックし、溝部１４内に密着層５２、Ｃｕ層５４及びＡｇ層５６から成る金属配線層５０を残す。Ａｇ層５６のエッチング

使用ガス　：　NO_2／O_2＝２０／２０sccm
マイクロ波パワー：　８５０Ｗ
ＲＦパワー　：　１０Ｗ
圧力　：　１．３Ｐａ
基板加熱温度　：　１００°Ｃ

Ｃｕ層５４及び密着層５２のエッチング

使用ガス　：　O_2／ClF_2＝１０／７０sccm
マイクロ波パワー：　１０００Ｗ
ＲＦパワー　：　３００Ｗ
圧力　：　０．５Ｐａ
基板加熱温度　：　３００°Ｃ

【０１０１】（実施例９）実施例９においては、実施例７の［工程－７１０］と［工程－７２０］との間に、溝部１４の側壁にＳｉＮから成るサイドウオール２６を形成する工程を更に含む。尚、その他の工程は実施例７と同様であり、詳細な説明は省略する。以下、実施例９のサイドウオール２６の形成工程を、図１４を参照して説明する。サイドウオール２６を形成することによって、絶縁層１２による密着層５２及びＣｕ層５４の酸化を防止することができる。

【０１０２】［サイドウオール２６の形成工程］溝部１４内を含む絶縁層１２上の全面にプラズマＣＶＤ法にてＳｉＮ層２６Ａを堆積させる（図１４の（Ａ）参照）。次に、ＳｉＮ層２６Ａを全面エッチバックする（図１４の（Ｂ）参照）。ＳｉＮ層２６Ａの形成条件及びエッチバックの条件を、例えば実施例３と同様とすることができる。これによって、溝部１４の側壁にサイドウオール２６が形成される。以降、実施例７の［工程－７２０］～［工程－７４０］を経て、図１４の（Ｃ）に示す配線構造を形成することができる。

【０１０３】（実施例１０）実施例９においてはＳｉＮから成るサイドウオール２６を溝部１４の側壁に形成した。これに対して、実施例１０においてはＡｇ（銀）からサイドウオールを形成する。尚、その他の工程は実施例７と同様であり、詳細な説明は省略する。以下、実施例１０のサイドウオールの形成工程を説明する。Ａｇから成るサイドウオールを形成することによって、絶縁層１２による密着層５２及びＣｕ層５４の酸化を防止することができる。

【０１０４】［Ａｇから成るサイドウオールの形成工程］溝部１４内を含む絶縁層１２上の全面にスパッタ法にてＡｇ層を堆積させる。次に、Ａｇ層を全面エッチバックする。Ａｇ層の形成条件及びエッチバックの条件を、以下に例示する。

Ａｇ層形成条件

使用ガス　：　Ａｒ＝１００sccm
パワー　：　４ｋＷ
圧力　：　０．４７Ｐａ
成膜温度　：　２００°Ｃ
膜厚　：　１００ｎｍ

Ａｇ層エッチバック条件

使用ガス　：　NO_2／O_2＝２０／２０sccm
マイクロ波パワー：　８５０Ｗ
ＲＦパワー　：　１０Ｗ
圧力　：　１．３Ｐａ
基板加熱温度　：　１００°Ｃ

こうして、図１４に示したと同様のサイドウオールを溝部１４の側壁に形成することができる。以降、実施例７の［工程－７２０］～［工程－７４０］を経て、図１４の（Ｃ）に示したと同様の配線構造を形成することができる。

【０１０５】（実施例１１）図１５に模式的な一部断面図を示す実施例１１の配線構造は、実施例７と若干異なり、半導体基板から成る基体１０上の第１の絶縁層１２Ａに形成された開口部１４Ａと、第１の絶縁層１２Ａ上に形成された第２の絶縁層１２Ｂに形成された溝部１４Ｂと、開口部１４Ａ及び溝部１４Ｂに埋め込まれた密着層５２、Ｃｕ層５４及びＡｇ層５６から成る金属配線層５０から構成されている。この場合、開口部１４Ａの側壁及び溝部１４Ｂの側部にＳｉＮから成るサイドウオール２６を形成してもよい。また、開口部１４Ａを金属配線層５０で埋め込むことによって、下層導体層（例えば、ソース・ドレイン領域３６）と溝部１４Ｂ内の配線５８とが電気的に接続される。

【０１０６】実施例１１の配線形成方法は、実施例７と若干異なり、予め半導体基板から成る基体１０上の第１の絶縁層１２Ａに開口部１４Ａを、また、第１の絶縁層１２Ａ上に形成された第２の絶縁層１２Ｂに溝部１４Ｂを形成した後、密着層５２、Ｃｕ層５４及びＡｇ層５６から成る金属配線層５０で開口部１４Ａ及び溝部１４Ｂを埋め込み配線構造を形成する。第２の絶縁層１２Ｂ上の金属配線層５０はケミカルメカニカルポリッシュ法にて除去される。以下、半導体装置等の模式的な一部断面図である図１６を参照して、実施例１１の配線形成方法を説明する。

【０１０７】［工程－１１００］Ｓｉ（１００）の半導体基板から成る基体１０上に、通常の方法で素子分離領域３０及びゲート領域３２を形成する。次いで、ＬＤＤ

イオン注入を行った後、ゲートサイドウオール３４を形成し、ソース・ドレイン領域形成のために、不純物イオン注入を行う。

【０１０８】［工程－１１１０］その後、SiO_2及びＢＰＳＧの２層から成る第１の絶縁層１２Ａを、例えばＣＶＤ法にて全面に形成し、リフロー処理を行い、第１の絶縁層１２Ａの平坦化を行う。

【０１０９】［工程－１１２０］次いで、第１の絶縁層１２Ａ上に、SiO_2から成る第２の絶縁層１２Ｂを形成する。

【０１１０】［工程－１１３０］その後、第２の絶縁層１２Ｂに溝部１４Ｂを形成する。

【０１１１】［工程－１１４０］更に、第１の絶縁層１２Ａに開口部１４Ａを形成する。次いで、開口部内にイオン注入を行うことにより、接合領域を形成させた後、活性化アニールを行う。

【０１１２】以上の工程は、実施例４の［工程－４００］～［工程－４４０］と同様とすることができる。

【０１１３】［工程－１１５０］次いで、実施例４の［工程－４５０］と同様に、ＳｉＮから成るサイドウオール２６を開口部１４Ａ及び溝部１４Ｂの側壁に形成してもよい。以上の工程によって、図１６の（Ａ）に示す構造が形成される。

【０１１４】［工程－１１６０］次に、下からＴｉ層／ＴｉＮ層から成る密着層５２を開口部１４Ａ及び溝部１４Ｂを含む第２の絶縁層１２Ｂ上にスパッタ法にて形成する。この工程は、実施例１の［工程－１２０］と同様とすることができる。

【０１１５】［工程－１１７０］その後、実施例７の［工程－７２０］と同様に、Ｃｕ層５４をスパッタ法にて全面に形成する。次いで、実施例７の［工程－７３０］と同様に、Ａｇ層５６をスパッタ法にて全面に形成する（図１６の（Ｂ）参照）。

【０１１６】［工程－１１８０］その後、実施例７の［工程－７４０］と同様に、ケミカルメカニカルポリッシュ法によって第２の絶縁層１２Ｂ上のＡｇ層５６、Ｃｕ層５４及び密着層５２を化学的及び機械的に研磨して除去し、溝部１４Ｂ内及び開口部１４Ａ内にＡｇ層５６、Ｃｕ層５４及び密着層５２を残し、金属配線層５０から成る接続孔及び配線を形成する（図１５参照）。即ち、開口部１４Ａ内に金属配線層５０が埋め込まれた接続孔５８Ａ（例えば、所謂コンタクトホール）が形成される。また、溝部１４Ｂに金属配線層５０が埋め込まれた配線５８が形成される。

【０１１７】尚、Ａｇ層５６、Ｃｕ層５４及び密着層５２から成る金属配線層５０をケミカルメカニカルポリッシュ法にて除去する代わりに、実施例８と同様にドライエッチング法にてエッチバックすることで除去することもできる。

【０１１８】（実施例１２）実施例１２は、実施例１１の変形である。実施例１２の配線構造は実施例１１と同様であるが、配線形成方法が実施例１１と相違する。即ち、第１の絶縁層１２Ａに設けられた開口部１４ＡをＣｕから成る金属配線材料で埋め込み接続孔５８Ａを完成させた後、その上に第２の絶縁層１２Ｂを堆積させ、かかる第２の絶縁層１２Ｂに溝部１４Ｂを形成する点が実施例１１と相違する。実施例１２においては、実施例１１の［工程－１１００］、［工程－１１１０］及び［工程－１１４０］は同様の工程であり、その他の工程が異なる。以下、図１７を参照して、実施例１２の方法を説明する。

【０１１９】

［工程－１２００］～［工程－１２２０］Ｓｉ（１００）の半導体基板から成る基体１０上に、通常の方法で素子分離領域３０及びゲート領域３２を形成する。次いで、ＬＤＤイオン注入を行った後、ゲートサイドウオール３４を形成し、ソース・ドレイン領域形成のために、不純物イオン注入を行う。その後、SiO_2及びＢＰＳＧの２層から成る第１の絶縁層１２Ａを、例えばＣＶＤ法にて全面に形成し、リフロー処理を行い、第１の絶縁層１２Ａの平坦化を行う。次いで、第１の絶縁層１２Ａに、レジストパターニング後ドライエッチングにて開口部１４Ａを形成し、開口部内にイオン注入を行うことにより、接合領域を形成させた後、活性化アニールを行う。これらの工程は、実施例４の［工程－１１００］、［工程－１１１０］及び［工程－１１４０］と同様とすることができる。次いで、ＳｉＮから成るサイドウオール（図示せず）を開口部１４Ａの側壁に形成してもよい。

【０１２０】［工程－１２３０］

［工程－１２２０］の後、実施例７の［工程－７１０］と同様の方法で、下からＴｉ／ＴｉＮから成る第１の密着層５２Ａを全面に形成する。次いで、実施例７の［工程－７２０］と同様の方法で、第１のＣｕ層５４Ａをスパッタ法にて全面に成膜し、第１の密着層５２Ａと第１のＣｕ層５４Ａから成る第１の金属配線層を形成する。

【０１２１】［工程－１２４０］その後、ケミカルメカニカルポリッシュ法にて第１の絶縁層１２Ａ上の第１の金属配線層を除去し、開口部１４Ａ内のみに第１の金属配線層５４Ａ，５２Ａを残す（図１７の（Ａ）参照）。ケミカルメカニカルポリッシュの条件は、実施例７の［工程－７４０］のＣｕ層のケミカルメカニカルポリッシュと同様とすることができる。これによって、開口部１４Ａに第１の金属配線層が埋め込まれた所謂コンタクトホール５８Ａが形成される。ケミカルメカニカルポリッシュ法の代わりに、実施例８と同様に、ドライエッチング法によるエッチバックにて開口部１４Ａ内のみに第１の金属配線層５４Ａ，５２Ａを残してもよい。

【０１２２】［工程－１２５０］次いで、全面にSiO_2から成る第２の絶縁層１２Ｂを形成する。第２の絶縁

層１２Ｂを、例えば実施例１１の［工程－１１２０］と同様の条件で形成することができる。その後、実施例１１の［工程－１１３０］と同様に、フォトリソグラフィ技術及びドライエッチング技術によって、第２の絶縁層１２Ｂに溝部１４Ｂを形成する。その後、必要に応じて、実施例１１の［工程－１１５０］と同様に、全面にプラズマＣＶＤ法にてＳｉＮ層を形成し、次いで、ＳｉＮ層を全面エッチバックし、これによって、溝部１４Ｂの側壁にＳｉＮから成るサイドウオール（図示せず）を形成しもてよい。

【０１２３】［工程－１２６０］次に、実施例７の［工程－７１０］と同様の方法で、厚さ３０ｎｍのＴｉから成る第２の密着層５２Ｂを溝部１４Ｂを含む第２の絶縁層１２Ｂ上にスパッタ法にて形成した後、実施例７の［工程－７３０］と同様の方法で、第２のＣｕ層５４Ｂをスパッタ法にて全面に成膜し、更に、その上にＡｇ層５６をスパッタ法にて成膜することによって、第２の密着層５２Ｂ、第２のＣｕ層５４Ｂ及びＡｇ層５６から成る第２の金属配線層を形成する。

【０１２４】［工程－１２７０］次いで、ケミカルメカニカルポリッシュ法によって第２の絶縁層１２Ｂ上の第２の金属配線層５６，５４Ｂ，５２Ｂを除去し、溝部１４Ｂ内にＡｇ層５６、第２のＣｕ層５４Ｂ及び第２の密着層５２Ｂを残し、配線５８を形成する（図１８の（Ｂ）参照）。ケミカルメカニカルポリッシュの条件は、実施例７の［工程－７４０］と同様とすることができる。

【０１２５】尚、ケミカルメカニカルポリッシュ法によって第２の絶縁層１２Ｂ上の第２の金属配線層５６，５４Ｂ，５２Ｂを除去する代わりに、実施例８と同様に、第２の金属配線層５６，５４Ｂ，５２Ｂをドライエッチング法にてエッチバックし、これによって、溝部１４Ｂ内にのみ第２の金属配線層５６，５４Ｂ，５２Ｂを残し、溝部１４Ｂ内に配線５８を形成することもできる。

【０１２６】（実施例１３）実施例７～実施例１２においては、半導体装置の配線構造を本発明の第２の態様に係る配線形成方法にて形成した。これに対して、実施例１３～実施例１５における半導体装置の配線構造は、本発明の第３の態様に係る配線形成方法にて形成する。

【０１２７】実施例１３の半導体装置の配線形成方法は、（イ）基体１０上に絶縁層１２を形成した後、絶縁層１２に溝部１４を形成する工程と、（ロ）溝部１４を含む絶縁層１２上に、下から密着層５２及びＣｕ層５４から成る多層の第１の金属配線層５０Ａを形成する工程と、（ハ）絶縁層１２上の第１の金属配線層５０Ａを除去し、溝部１４内に第１の金属配線層５０Ａを残す工程と、（ニ）絶縁層１２上及び第１の金属配線層５０Ａ上に、Ａｇ層から成る第２の金属配線層５０Ｂを形成する工程と、（ホ）絶縁層１２上の第２の金属配線層５０Ｂを除去し、溝部１４内に第２の金属配線層５０Ｂを残す工程から成る。

【０１２８】密着層５２、Ｃｕ層５４及び第２の金属配線層５０Ｂの形成はスパッタ法にて行う。また、（ハ）の工程における絶縁層１２上の第１の金属配線層５０Ａの除去、並びに（ホ）の工程における絶縁層１２上の第２の金属配線層５０Ｂの除去は、金属配線層５０のケミカルメカニカルポリッシュ工程から成る。SiO_2から成る絶縁層１２をストッパーとして機能させることにより、ケミカルメカニカルポリッシュに対する第１及び第２の金属配線層５０Ａ，５０Ｂと絶縁層１２の選択比を無限大まで設定することが可能となる。

【０１２９】本発明の第３の態様に係る配線形成方法においては、本発明の第２の態様に係る配線形成方法よりも一層確実にＣｕ層５４をＡｇ層から成る第２の金属配線層５０Ｂで被覆することができる。

【０１３０】以下、半導体装置等の模式的な一部断面図である図１８及び図１９を参照して、実施例１３の配線形成方法を具体的に説明する。

【０１３１】［工程－１３００］例えば半導体基板から成る基体１０上にSiO_2から成る絶縁層１２を形成する。絶縁層１２の形成条件を、例えば実施例１の［工程－１００］と同様とすることができる。その後、フォトリソグラフィ技術及びドライエッチング技術によって、絶縁層１２に溝部１４を形成する。尚、溝部１４は図１８の紙面に垂直な方向に延びている。ドライエッチングの条件を、実施例１の［工程－１１０］と同様とすることができる。

【０１３２】［工程－１３１０］次に、下からＴｉ層５２Ａ／ＴｉＮ層５２Ｂから成る密着層５２を溝部１４を含む絶縁層１２上にスパッタ法にて形成する。密着層５２を、例えば実施例１の［工程－１２０］と同様とすることができる。

【０１３３】［工程－１３２０］その後、銅（Ｃｕ）層５４をスパッタ法にて全面に形成する（図１８の（Ａ）参照）。Ｃｕ層５４の形成を、実施例７の［工程－７２０］と同様とすることができる。こうして、溝部１４を含む絶縁層１２上に、下から密着層５２及びＣｕ層５４から成る多層の第１の金属配線層５０Ａを形成することができる。

【０１３４】［工程－１３３０］次に、ケミカルメカニカルポリッシュ法によって絶縁層１２上のＣｕ層５４及び密着層５２を化学的及び機械的に研磨して除去し、溝部１４内にＣｕ層５４及び密着層５２から成る第１の金属配線層５０Ａを残す（図１８の（Ｂ）参照）。ケミカルメカニカルポリッシュには、図４に示す研磨装置を用いる。ケミカルメカニカルポリッシュの条件を、実施例１３と同様とすることができる。Ｃｕ層５４及び密着層５２のケミカルメカニカルポリッシュ法による除去には$K_4Fe(CN)_6+H_2O$を用いる。

【０１３５】［工程－１３４０］その後、銀（Ａｇ）層

から成る第２の金属配線層５０Ｂをスパッタ法にて全面に形成する（図１９の（Ａ）参照）。Ａｇ層の形成を、実施例１３の［工程－７３０］と同様とすることができる。こうして第１の金属配線層５０Ａの表面がＡｇ層から成る第２の金属配線層５０Ｂで被覆される。

【０１３６】［工程－１３５０］次に、ケミカルメカニカルポリッシュ法によって絶縁層１２上のＡｇ層から成る第２の金属配線層５０Ｂを化学的及び機械的に研磨して除去し、溝部１４内にＡｇ層から成る第２の金属配線層５０Ｂを残し、第１及び第２の金属配線層５０Ａ，５０Ｂから成る配線を形成する（図１９の（Ｂ）参照）。ケミカルメカニカルポリッシュの条件は、実施例１３と同様とすることができる。尚、Ａｇ層のケミカルメカニカルポリッシュ法による除去にはI_2＋ＫＩの混合水溶液を用いる。

【０１３７】実施例１３においては、従来の配線形成方法のように金属配線層のレジストパターニング処理及びドライエッチング処理が不要となり、レジストパターニング時の光の散乱の問題、エッチングが不均一となる問題を回避することができる。また、配線上の絶縁膜の形成及びかかる絶縁膜の平坦化処理も不要である。また、第１の金属配線層５０Ａの表面は第２の金属配線層５０Ｂによって一層確実に被覆されているので、第１の金属配線層５０Ａを構成するＣｕ層５４の酸化を防止することができる。

【０１３８】実施例１３においては、第１の金属配線層５０Ａ及び第２の金属配線層５０Ｂの除去を専らケミカルメカニカルポリッシュ法にて行ったが、実施例８と同様にドライエッチング法によるエッチバックにて除去することもできる。

【０１３９】また、実施例１３にて説明した本発明の第３の態様に係る半導体装置の配線形成方法と、実施例９あるいは実施例１０にて説明したサイドウオールの形成とを組み合わせることもできる。更には、実施例１１あるいは実施例１２におけるＡｇ層５６の代わりに、実施例１３にて説明した配線形成方法を適用することもできる。

【０１４０】（実施例１４）実施例１１におけるＡｇ層５６の代わりに、実施例１３にて説明した配線形成方法を適用する場合の工程のフローのみを、以下に説明する。尚、第１及び／又は第２の金属配線層をケミカルメカニカルポリッシュ法にて除去する代わりに、実施例８と同様にドライエッチング法にてエッチバックすることで除去することもできる。

【０１４１】［工程－１４００］基体上への、素子分離領域、ゲート領域の形成。ＬＤＤイオン注入。ゲートサイドウオールの形成。ソース・ドレイン領域形成のための不純物イオン注入。

［工程－１４１０］SiO_2及びＢＰＳＧの２層から成る第１の絶縁層の形成及びリフロー処理。

［工程－１４２０］第１の絶縁層上へのSiO_2から成る第２の絶縁層の形成。

［工程－１４３０］第２の絶縁層への溝部の形成。

［工程－１４４０］第１の絶縁層への開口部の形成。

［工程－１４５０］Ｔｉ層／ＴｉＮ層から成る密着層の開口部及び溝部を含む第２の絶縁層上へのスパッタ法による形成。

［工程－１４６０］密着層上へのスパッタ法によるＣｕ層の形成。

［工程－１４７０］ケミカルメカニカルポリッシュによる第２の絶縁層上のＣｕ層の除去。

［工程－１４７０］全面に、スパッタ法によるＡｇ層から成る第２の金属配線層の形成。

［工程－１４８０］ケミカルメカニカルポリッシュ法による第２の絶縁層上の第２の金属配線層の除去。

【０１４２】（実施例１５）実施例１２におけるＡｇ層５６の代わりに、実施例１３にて説明した配線形成方法を適用する場合の工程のフローのみを、以下に説明する。尚、第１及び／又は第２の金属配線層をケミカルメカニカルポリッシュ法にて除去する代わりに、実施例８と同様にドライエッチング法にてエッチバックすることで除去することもできる。

【０１４３】［工程－１５００］基体上への、素子分離領域、ゲート領域の形成。ＬＤＤイオン注入。ゲートサイドウオールの形成。ソース・ドレイン領域形成のための不純物イオン注入。

［工程－１５１０］SiO_2及びＢＰＳＧの２層から成る第１の絶縁層の形成及びリフロー処理。

［工程－１５２０］第１の絶縁層への開口部の形成。

［工程－１５３０］第１の絶縁層上への第１の密着層及び第１のＣｕ層から成る第１の金属配線層のスパッタ法による形成。

［工程－１５４０］ケミカルメカニカルポリッシュ法による第１の絶縁層上の第１の金属配線層の除去。これによって、開口部に第１の金属配線層が埋め込まれた所謂コンタクトホールを形成。

［工程－１５５０］全面に、SiO_2から成る第２の絶縁層の形成。第２の絶縁層への溝部の形成。

［工程－１５６０］第２の絶縁層上への第２の密着層及びＣｕ層のスパッタ法による形成。

［工程－１５７０］ケミカルメカニカルポリッシュによる第２の絶縁層上のＣｕ層及び第２の密着層の除去。

［工程－１５８０］全面に、スパッタ法によるＡｇ層から成る第２の金属配線層の形成。

［工程－１５９０］ケミカルメカニカルポリッシュ法による第２の絶縁層上の第２の金属配線層の除去。

【０１４４】以上、本発明を好ましい実施例に基づき説明したが、本発明はこれらの実施例に限定されるものではない。実施例にて用いた各種材料や条件は例示であり、適宜変更することができる。場合によっては、溝部

１４，１４Ｂの代わりに開口部を形成することができる。

【０１４５】絶縁層は専らＳｉO_2あるいはＳｉO_2とＢＰＳＧの組み合わせから成るものとして説明したが、これらの代わりに、ＢＰＳＧ、ＰＳＧ、ＢＳＧ、ＡｓＳＧ、ＰｂＳＧ、ＳｂＳＧ、ＳＯＧ、ＳｉＯＮあるいはＳｉＮ等の公知の絶縁材料、あるいはこれらの絶縁層を積層したものから構成することができる。

【０１４６】実施例１～実施例６においては、Ａｇ層２０の形成は、Ａg_2CO_3を原料として用いた化学気相析出法にて行ったが、その代わりに、ＡgNO_2、ＡｇＢｒ若しくはＡｇＩを原料として用いた化学気相析出法にて行うことができる。これらの場合のＣＶＤ条件、及び図３に示したＣＶＤ装置において第１及び第２のヒーター２０６，２１０によって配管２０４及びＣＶＤチャンバ導入部２０８内を流れる原料ガスの加熱条件を以下に例示し、併せて反応式を示す。

【０１４７】原料：ＡgNO_2
原料源温度　：　１５０°Ｃ
使用ガス　　：　ＡgNO_2／Ａｒ／H_2＝１０／２５／１０００sccm
圧力　　：　２．６×10^3Ｐａ
基板加熱温度：　４５０°Ｃ
ガス加熱条件：　１４０°Ｃ以上
反応式　　：　２ＡgNO_2＋７H_2→２Ａｇ＋２NH_3↑＋４H_2O↑

【０１４８】原料：ＡｇＢｒ
原料源温度　：　４５０°Ｃ
使用ガス　　：　ＡｇＢｒ／Ａｒ／H_2＝１０／７５／１０００sccm
圧力　　：　２．６×10^3Ｐａ
基板加熱温度：　５００°Ｃ
ガス加熱条件：　４３４°Ｃ以上
パワー　　：　５００Ｗ　（プラズマＣＶＤ）
反応式　　：　２ＡｇＢｒ＋H_2→２Ａｇ＋２ＨＢｒ↑

【０１４９】原料：ＡｇＩ
原料源温度　：　５６０°Ｃ
使用ガス　　：　ＡｇＩ／Ａｒ／H_2＝１０／１００／１０００sccm
圧力　　：　２．６×10^3Ｐａ
基板加熱温度：　６００°Ｃ
ガス加熱条件：　５５２°Ｃ以上
パワー　　：　５００Ｗ　（プラズマＣＶＤ）
反応式　　：　２ＡｇＩ＋H_2→２Ａｇ＋２ＨＩ↑

【０１５０】実施例７～実施例１５において、Ｃｕ層及び／又はＡｇ層をスパッタ法にて形成する代わりに、ＣＶＤ法にて形成することができる。ＣＶＤ法によるＣｕ層の形成条件を以下に例示する。
使用ガス　　：　Ｃｕ（ＨＦＡ）$_2$／H_2＝１０／１００sccm
圧力　　：　２．６×10^3Ｐａ
基板加熱温度：　３５０°Ｃ
パワー　　：　５００Ｗ
尚、ＨＦＡとは、ヘキサフルオロアセチルアセトネートの略である。

【０１５１】密着層を、Ｔｉ層／ＴｉＮ層の代わりに、Ｔｉ層、あるいはＴｉＮ層から構成することもできる。この場合の、Ｔｉ層又はＴｉＮ層の形成条件は、実施例１の［工程－１２０］にて説明したＴｉ層１８Ａ、ＴｉＮ層１８Ｂの形成条件と同様とすることができる。あるいは又、密着層を、下からＡｇ層／Ｔｉ層の２層構造とすることもできる。この場合、Ａｇ層を、以下の条件のスパッタ法にて形成することができる。また、Ｔｉ層の形成条件は、実施例１の［工程－１２０］にて説明したＴｉ層１８Ａの形成条件と同様とすることができる。
Ａｇ層のスパッタ条件
使用ガス　　：　Ａｒ＝１００sccm
パワー　　：　４ｋＷ
圧力　　：　０．４７Ｐａ
成膜温度　　：　２００°Ｃ
膜厚　　：　５０ｎｍ

【０１５２】密着層を構成するＴｉＮの代わりに、ＴｉＯＮやＴｉＷを用いることもできる。また、場合によっては、溝部の形成、サイドウオールの形成、密着層の形成の順序を変更して、溝部の形成、密着層の形成、サイドウオールの形成の順とすることもできる。また、Ｔｉ、ＴｉＮ等の密着層を構成する金属層又は金属化合物層は、ＣＶＤ等の成膜法で形成することができる。

【０１５３】基体としては、シリコン半導体基板、あるいはソース・ドレイン領域が形成された半導体基板の他にも、ＭｇＯ基板、ＧａＡｓ基板、超伝導トランジスタ基板、下層配線層が形成された絶縁層、接続孔（コンタクトホール、ビヤホール、スルーホール）を形成して電気的接続を形成する必要があるゲート電極等の各種素子部、薄膜トランジスタを作製するための各種基板上に形成されたシリコン層等を挙げることができる。

【０１５４】実施例６においては、所謂ブランケットタングステンＣＶＤ法を用いて開口部１４Ａ内にタングステンプラグを形成したが、代わりに、所謂タングステン選択ＣＶＤ法にて開口部１４Ａ内にタングステンプラグを形成してもよい。この場合の条件を、例えば以下のとおりとすることができる。使用ガス　：　WF_6／SiH_4／H_2／Ａｒ＝１０／７／１０００／１０ sccm
温　度　　：　２６０°Ｃ
圧　力　　：　２６Ｐａ

【０１５５】本発明は、ＭＯＳ半導体装置以外の他の半導体装置（例えば、バイポーラトランジスタ、ＣＣＤ）にも適用できる。

【０１５６】スパッタ法は、マグネトロンスパッタリング装置、ＤＣスパッタリング装置、ＲＦスパッタリング装置、ＥＣＲスパッタリング装置、また基板バイアスを印加するバイアススパッタリング装置等各種のスパッタリング装置にて行うことができる。

【０１５７】本発明の第１の態様に係る配線構造においてはＡｇ層の下に、また、本発明の第２の態様に係る配線構造においてはＣｕ層の下に、あるいは又、密着層の下の配線層若しくは接続孔に、Ｍｏ、Ｔｉ等の高融点金属、又は、ＴｉＷ、ＺｒＮ、Ｗ、ＷＣ、ＴｉＣ、その他$MoSi_2$、WSi_2、$TiSi_2$等のシリサイド等を単層若しくは各種組み合わせた多層膜を形成することができる。

【０１５８】

【発明の効果】本発明においては、配線を形成するためのフォトリソグラフィ技術及びドライエッチング技術による金属配線層のパターニング工程が不要である。従って、従来のフォトリソグラフィ技術における光の乱反射、あるいはドライエッチングにおけるエッチングの不均一性やコロージョンの問題を回避することができる。

【０１５９】また、微細な配線を有する半導体装置の作製において、従来のように配線上に形成された絶縁膜の形成、あるいはかかる絶縁膜の研磨を行わずに、配線を含む絶縁層の完全なる平坦化が可能となる。従来のSiO_2系絶縁膜は研磨における選択性が乏しいために研磨の制御性が乏しかったが、金属配線層の研磨は絶縁層に対する選択性が大きいので、研磨の制御性も格段に向上する。

【０１６０】更に、溝部又は開口部内のみに金属配線層を残すために、ケミカルメカニカルポリッシュ法あるいはドライエッチング法によるエッチバックを採用することによって、従来の技術を基本的にはそのまま用いることができ、半導体装置の製造コストが増加することもない。

【０１６１】尚、溝部又は開口部内にサイドウオールを形成することで、金属配線層の酸化を防止でき、しかも金属配線層によって溝部又は開口部を安定して埋め込むことができる。

【０１６２】本発明の第１の態様に係る配線構造及び配線形成方法においては、Ａｌ系合金より耐エレクトロマイグレーション性を有するＡｇ層から配線構造を構成するので半導体素子の信頼性が従来より向上する。更に、ＡｇはＡｌ系合金より抵抗が低いので半導体素子の応答スピードが期待できる。

【０１６３】本発明の第２の態様に係る配線構造、並びに第２及び第３の態様に係る配線形成方法においては、Ａｌ系合金より耐エレクトロマイグレーション性を有するＣｕ層から金属配線層を構成するので半導体素子の信頼性が従来より向上する。また、Ｃｕ層の表面はＡｇ層で被覆されているので、Ｃｕ層の酸化を防ぐと同時に、Ａｇの低抵抗性によって配線抵抗を低く保つことができる。従来、Ｃｕは酸化等の問題でプロセス限定の必要があったが、酸素雰囲気の熱処理等のプロセスを用いることが可能になる。

【０１６４】本発明の銀薄膜形成方法により、ＡｇのＣＶＤが可能となり、溝部や開口部へのＡｇの完全埋め込みが可能となる。

【０１６５】更には、本発明のＣＶＤ装置においては、ＣＶＤチャンバへのソース供給配管及びＣＶＤチャンバの接続部を高い温度に保持できるので、安定して原料ガスを供給することができる。

【図面の簡単な説明】

【図１】実施例１の半導体装置の配線構造の模式的な図である。

【図２】実施例１の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図３】本発明のＣＶＤ装置の模式図である。

【図４】本発明の実施に適した研磨装置の模式図である。

【図５】実施例３のサイドウオール形成工程を説明するための半導体素子等の模式的な一部断面図である。

【図６】実施例４の半導体装置の配線構造の模式的な図である。

【図７】実施例４の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図８】図７に引き続き、実施例４の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図９】実施例５の配線形成方法の工程を説明するための半導体素子等の模式的な一部断面図である。

【図１０】図９に引き続き、実施例５の配線形成方法の工程を説明するための半導体素子等の模式的な一部断面図である。

【図１１】実施例６の配線形成方法の工程を説明するための半導体素子等の模式的な一部断面図である。

【図１２】実施例７の半導体装置の配線構造の模式的な図である。

【図１３】実施例７の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図１４】実施例９のサイドウオール形成工程を説明するための半導体素子等の模式的な一部断面図である。

【図１５】実施例１１の半導体装置の配線構造の模式的な図である。

【図１６】実施例１１の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図１７】実施例１２の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図１８】実施例１３の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図１９】図１８に引き続き、実施例１３の配線形成方

法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図２０】従来の半導体素子の製造プロセス例における各工程を説明するための半導体装置等の模式的な一部断面図である。

【図２１】図２０に引き続き、従来の半導体素子の製造プロセス例における各工程を説明するための半導体装置等の模式的な一部断面図である。

【図２２】従来の半導体素子の製造プロセスの別の例における各工程を説明するための半導体装置等の模式的な一部断面図である。

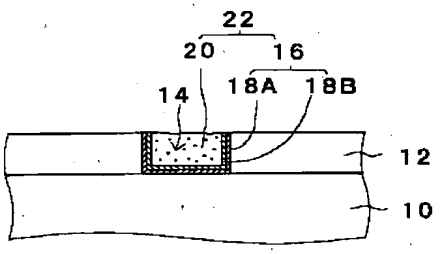
【図２３】従来の半導体素子の製造プロセスにおける問題点を説明するための図である。

【符号の説明】

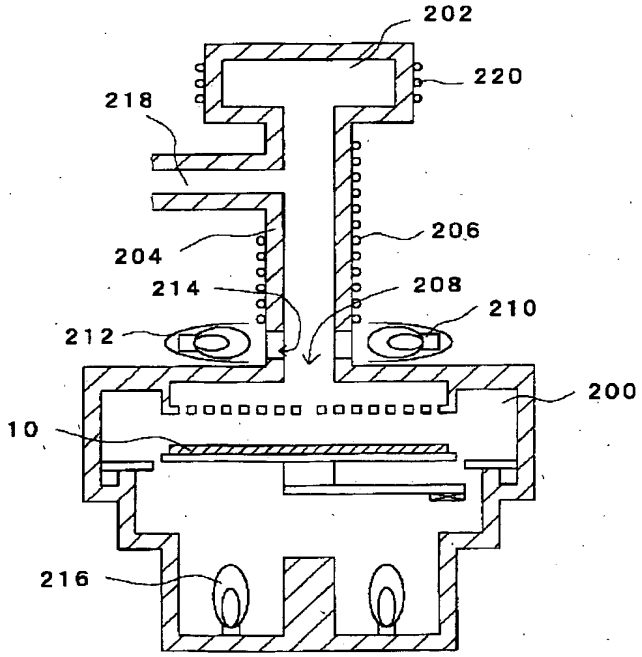
１０　基体
１２，１２Ａ，１２Ｂ　絶縁層
１４，１４Ｂ　溝部
１４Ａ　開口部
１６，１６Ａ，１６Ｂ　密着層
１８Ａ　Ｔｉ層
１８Ｂ　ＴｉＮ層
２０　Ａｇ層
２２　金属配線層
２４　配線
２４Ａ　接続孔
２６Ａ　ＳｉＮ層
２６　サイドウオール
３０　素子分離領域
３２　ゲート領域
３４　ゲートサイドウオール
３６　ソース・ドレイン領域
４０　バリア層
４２　タングステン層
５０　金属配線層
５０Ａ　第１の金属配線層
５０Ｂ　第２の金属配線層
５２，５２Ａ，５２Ｂ　密着層
５４，５４Ａ，５４Ｂ　Ｃｕ層
５６　Ａｇ層
５８　配線
５８Ａ　接続孔
２００　ＣＶＤチャンバ
２０２　原料源
２０４　配管
２０６　第１のヒーター
２０８　ＣＶＤチャンバ導入部
２１０　第２のヒーター
２１４　窓
２１６　ランプ加熱装置
２１８　不活性ガス導入部

【図１】

（実施例１の配線構造）

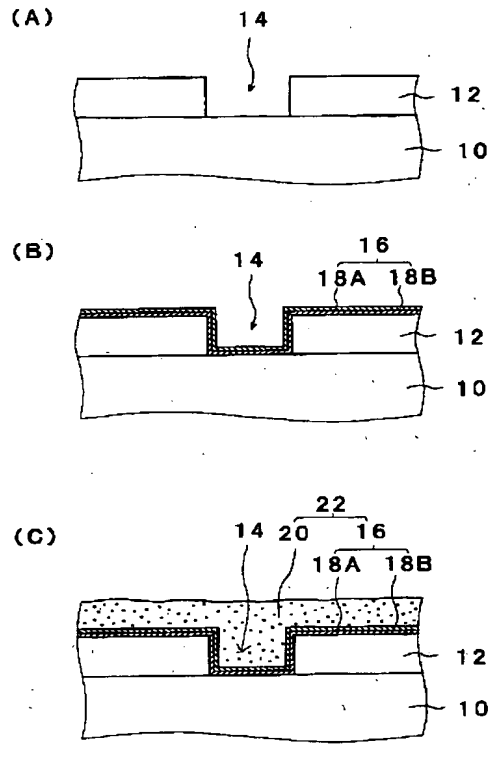


【図３】



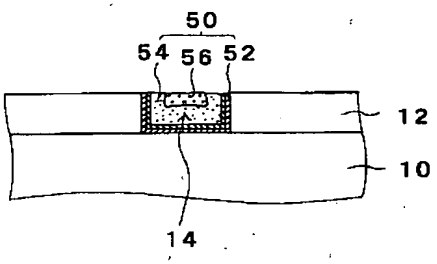
【図２】

（実施例１の配線形成方法）

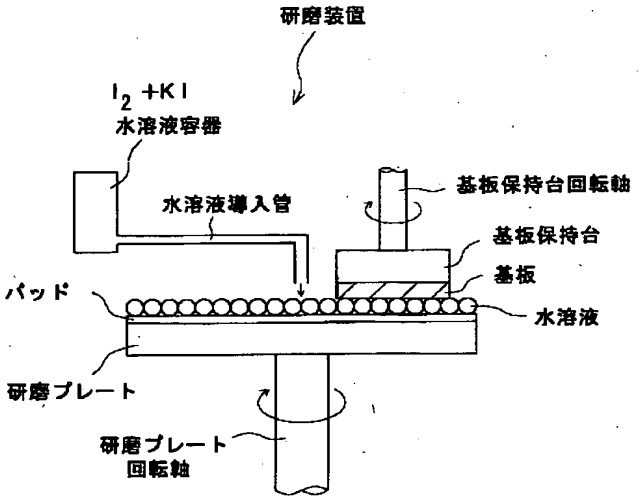


【図１２】

（実施例７の配線構造）

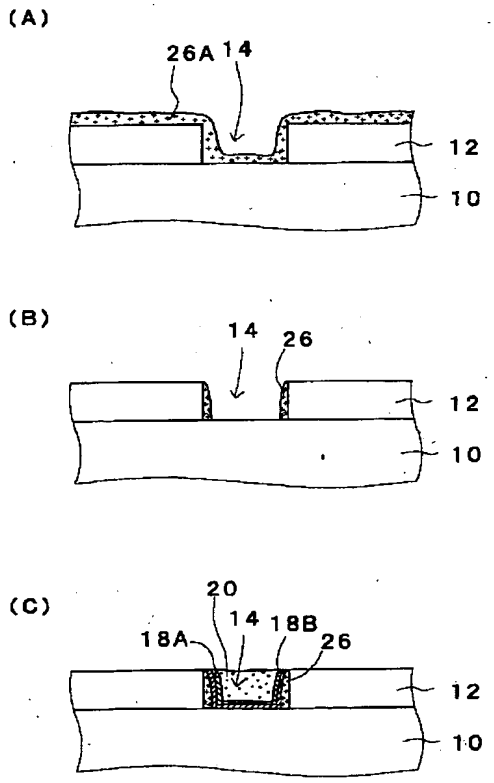


【図４】



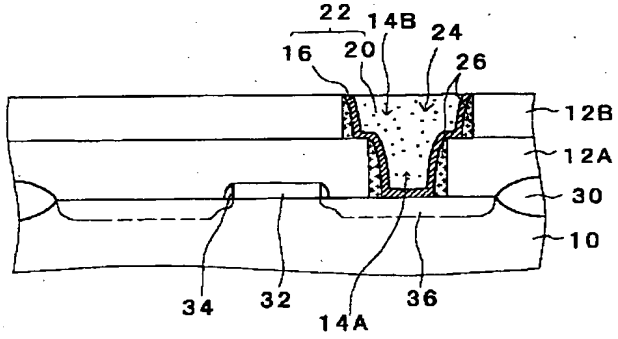
【図５】

（実施例３の配線形成方法）



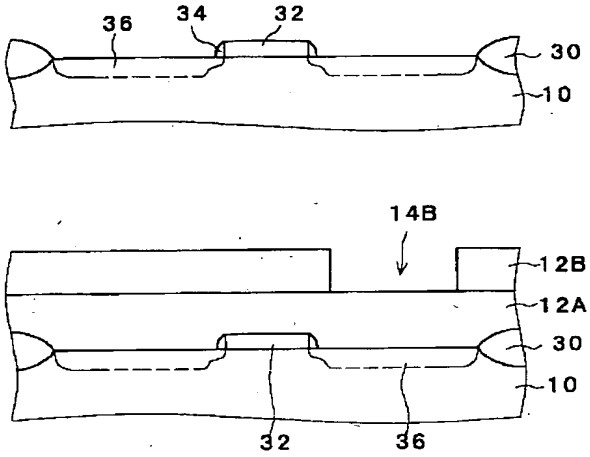
【図６】

（実施例４の配線構造）



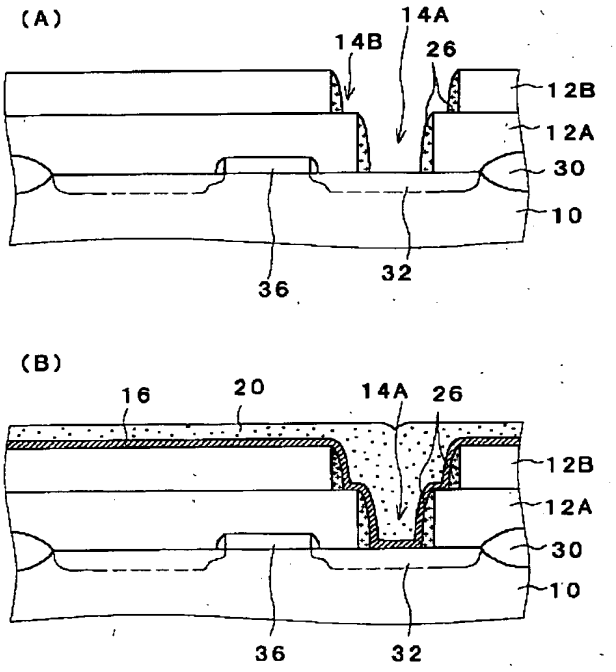
【図７】

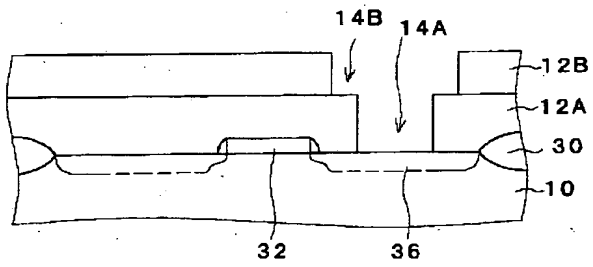
（実施例４の配線形成方法）



【図８】

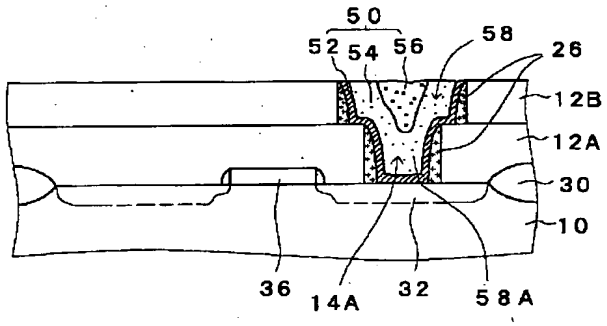
（実施例４の配線形成方法）　（続き）





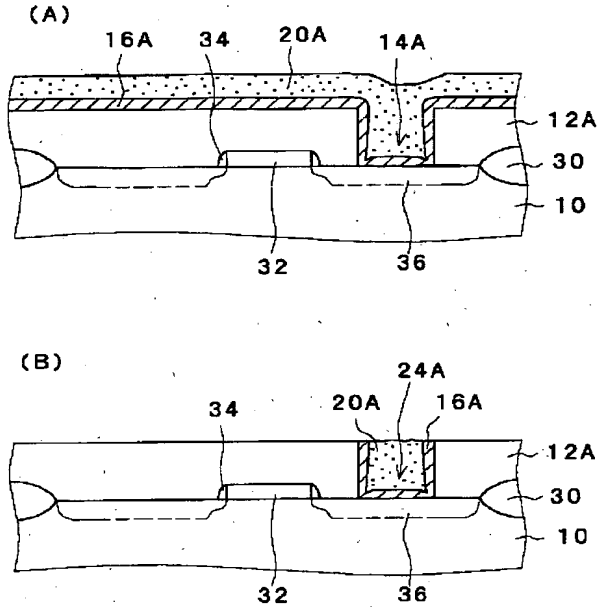
【図１５】

（実施例１１の配線構造）



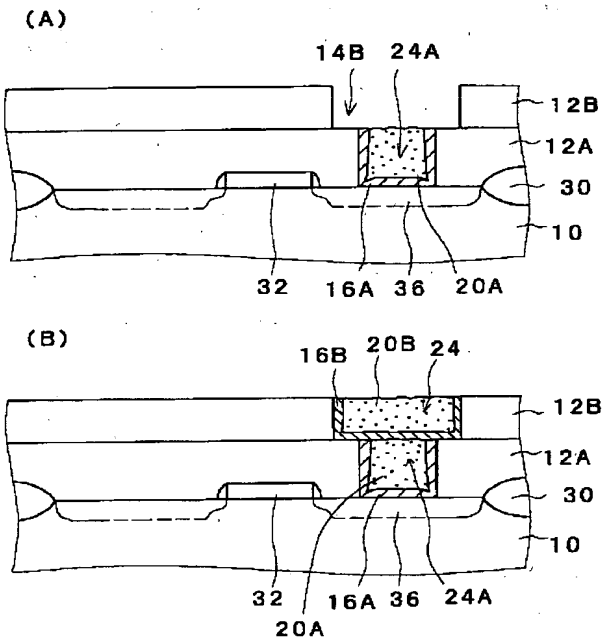
【図９】

（実施例５の配線形成方法）



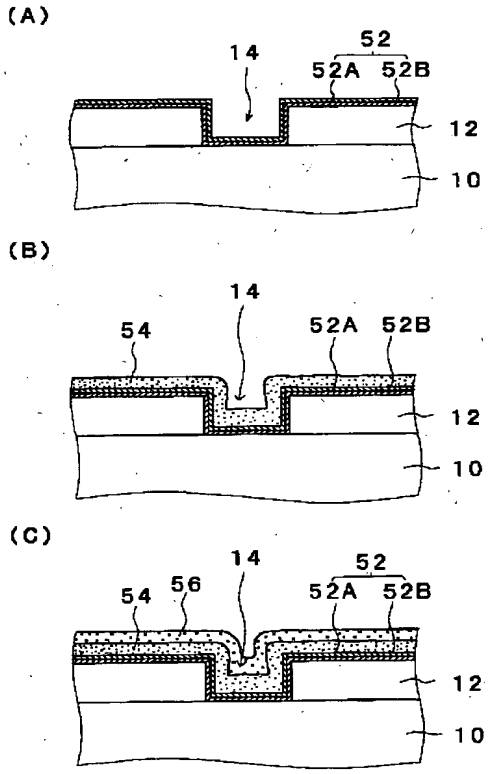
【図１０】

（実施例５の配線形成方法）　（続き）



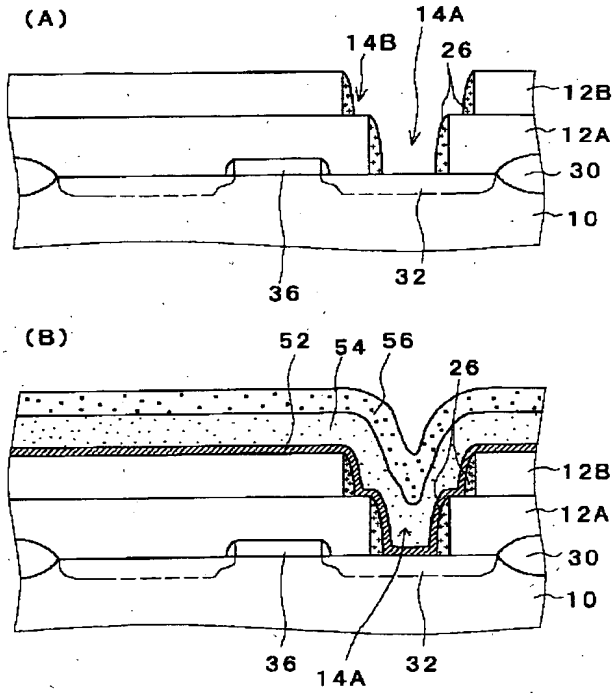
【図１３】

（実施例７の配線形成方法）



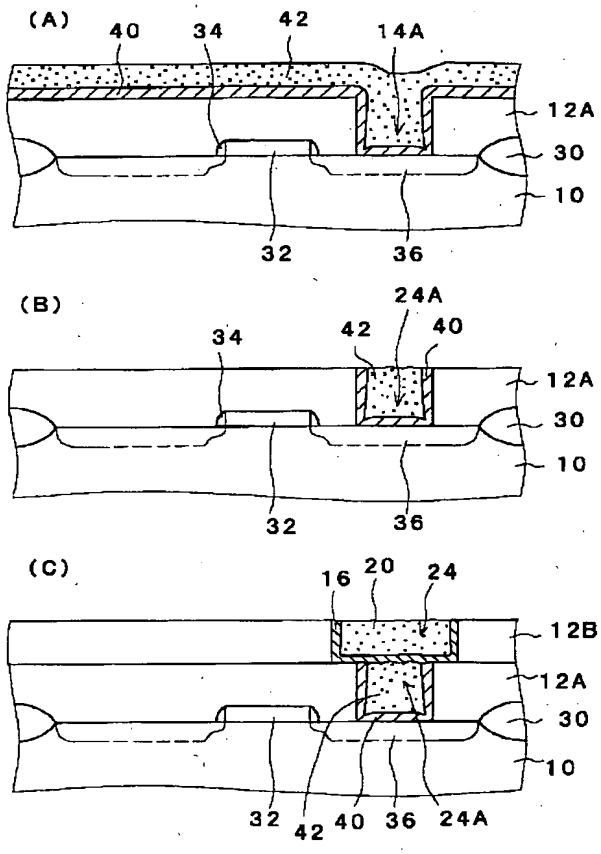
【図１６】

（実施例１１の配線形成方法）



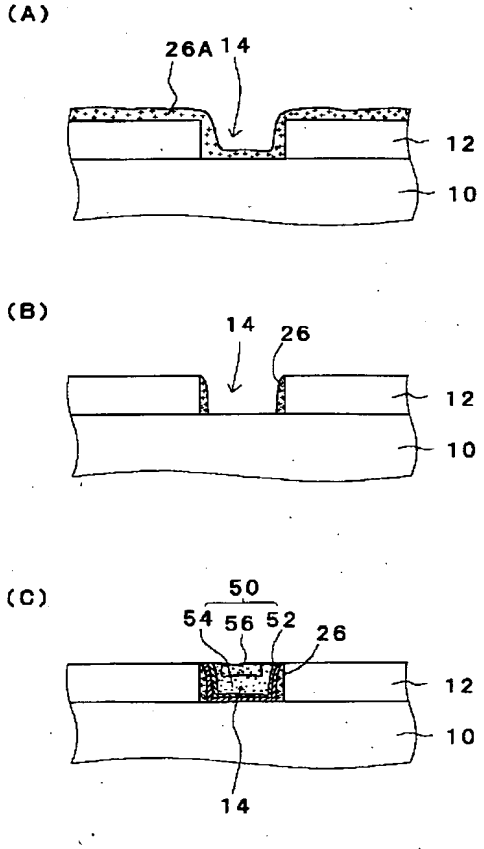
【図１１】

（実施例６の配線形成方法）



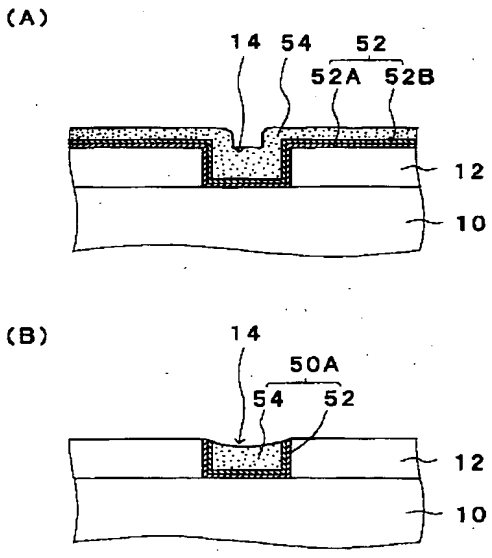
【図１４】

（実施例９の配線形成方法）



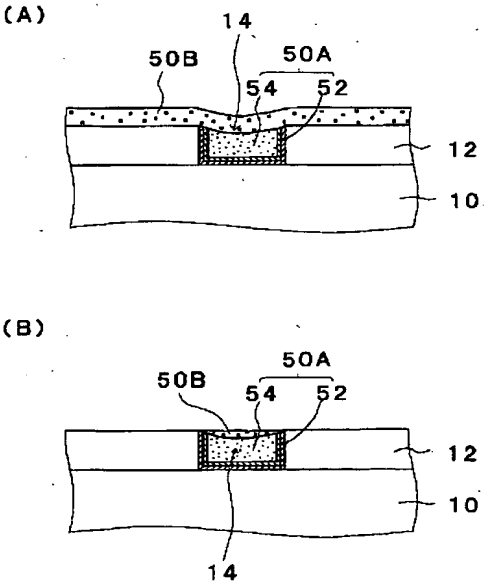
【図１８】

（実施例１３の配線形成方法）



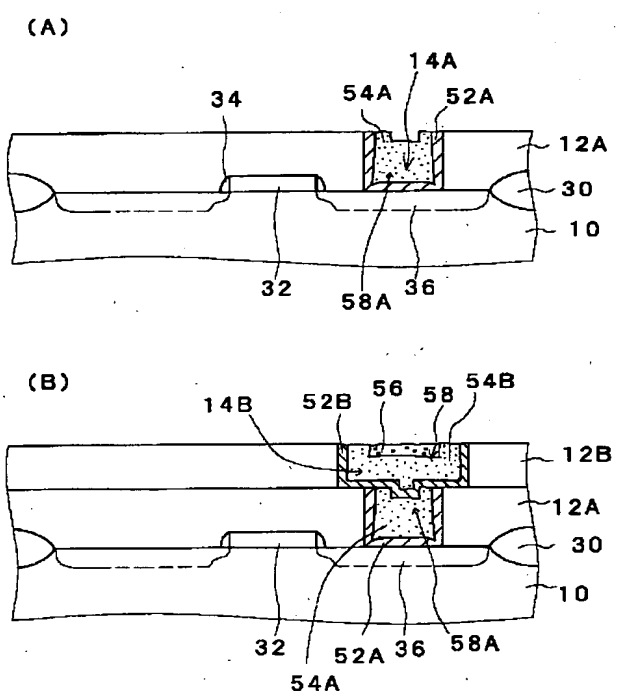
【図１９】

（実施例１３の配線形成方法）　（続き）



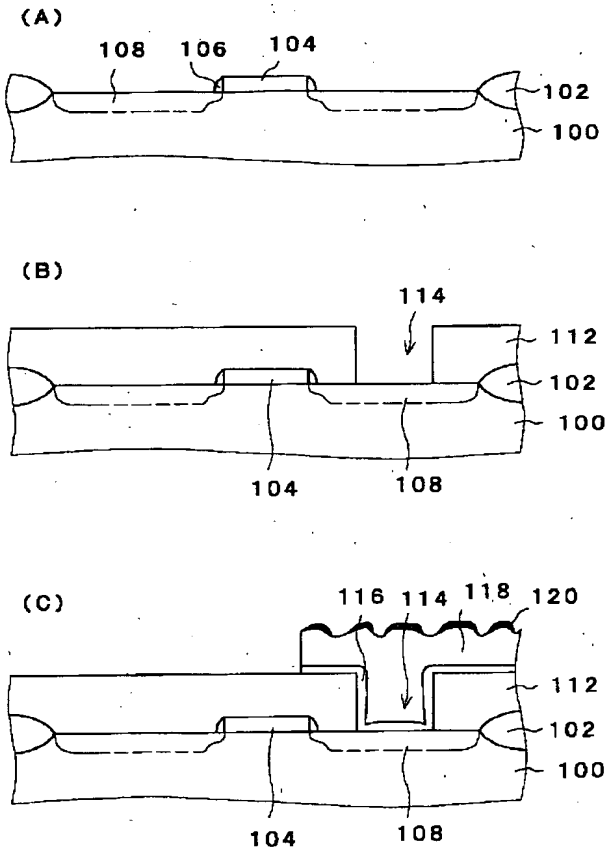
【図１７】

（実施例１２の配線形成方法）



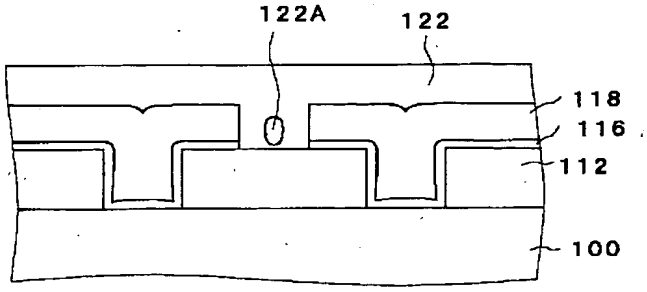
【図２０】

（従来技術，その１）



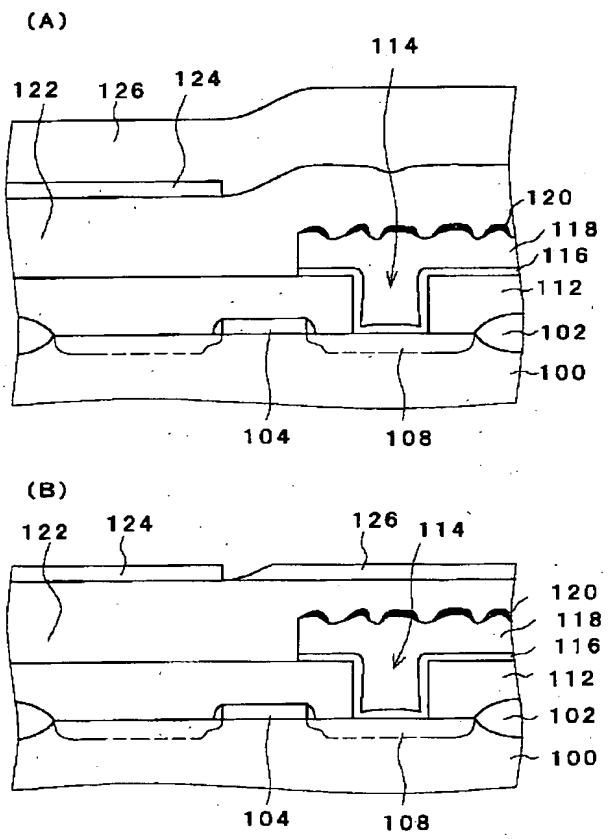
【図２３】

（従来技術における問題点）



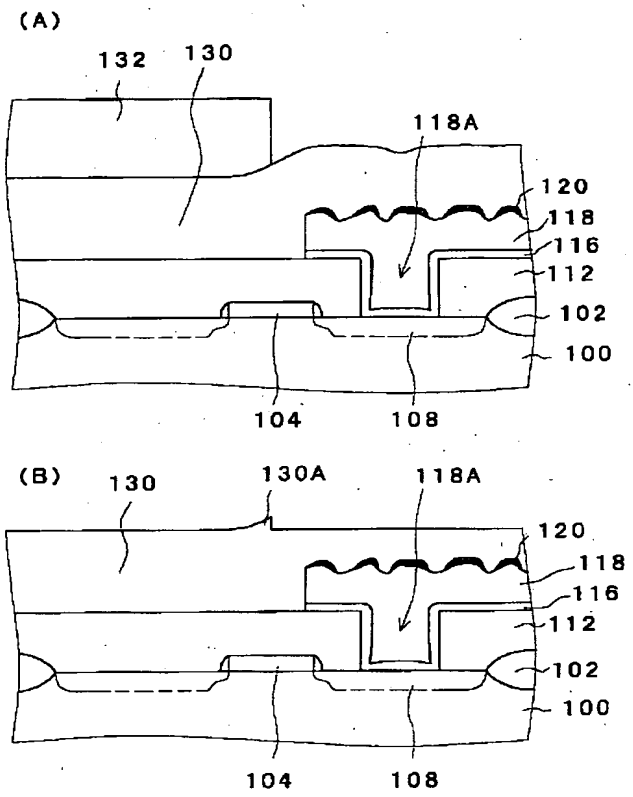
【図２１】

（従来技術，その１）　（続き）



【図２２】

（従来技術，その２）



フロントページの続き

(51) Int. Cl. ⁶	識別記号	庁内整理番号	Ｆ Ｉ	技術表示箇所
Ｈ０１Ｌ　21/3205				